88-2SIOJP

Dual Serial Port with Jump-Start and PROM

User's Guide

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Revision History

Manual	Board	Date	Author	Notes
2.00	C	16 AUG 2016	M. Eberhard	First released version

TABLE OF CONTENTS

INTRODUCTION

The 88-2SIOJP is an enhanced dual serial port board designed for the MITS Altair computer, and provides the following functions:

1. Two serial ports that are software and hardware compatible with the MITS 88-2SIO, with some important enhancements
2. One 2716 EPROM/2816A EEPROM socket, providing 2K-bytes of PROM storage, with write capability for EEPROMs
3. Altair-compatible automatic PROM disable, allowing the Altair to have a full 65K-bytes[1] of RAM for software such as Basic
4. Power-on/reset jump-start that is compatible with memory boards (such as all MITS memory boards) that do not support the S-100 Phantom signal, as well as memory boards that do support Phantom
5. Improved power-on clear circuit, eliminating the need to toggle the Reset switch on the Altair 8800 and 8800a

Serial Ports

The serial ports are designed around the Motorola 68B50 ACIA. The data rate for each serial port is set by a DIP switch, allowing communication from 110 baud through 76.8K baud. (For comparison, the maximum data rate for the MITS 88-2SIO is 9600 baud.)

Either port can be set up for RS-232 (with optional hardware handshaking), Teletype (20 mA current loop), or TTL communication.

The serial ports operate without any wait states. (The MITS 88-2SIO generates a wait state for every IN instruction.)

The 88-2SIOJP can provide regulated +12V and -12V to an external device.

EPROM and EEPROM

The EPROM socket supports both 2716 EPROMs and 2816A EEPROMs. The starting address for the EPROM is set with a DIP switch.

PROM access requires zero wait states.

If a 2816A EEPROM is installed, then writing to the EEPROM is enabled and disabled with a jumper.

The EPROM can be completely disabled with a DIP switch.

Automatic EPROM Disable

When the Automatic EPROM Disable feature is enabled, the EPROM is available to the CPU after reset and until the first IN instruction from port 0FFh (which is the Altair front panel’s switch register). Once the CPU inputs from this port, the EPROM is no longer available,

[1] The full address range of an Altair is 65,536 bytes. This is abbreviated as 65K in this manual. 65,536 bytes is sometimes referred to as 64K, since it is 1K (1024 bytes) times 64.

and any other RAM at the same address becomes available to the CPU. This feature can be disabled with a DIP switch. (This is similar to the automatic EPROM disable feature of later MITS 8800b Turnkey Modules, and allows e.g. Altair Basic to run in 65K of RAM.)

Jump-Start

When the Jump-Start feature is enabled, the 88-2SIOJP forces a jump to the jump-start address (which is set by a DIP switch) upon Reset. This jump-start is implemented in one of two (DIP-switch selectable) ways:

1) The 88-2SIOJP disables the status signals generated by the Altair CPU board, and generates replacement status signals with MEMR held low, so that other memory boards do not respond. This method works with almost all memory boards, including SRAM, DRAM, and PROM boards made by MITS.

2) The 88-2SIO generates a PHANTOM signal on the bus, which will disable many S-100 memory boards, though not any MITS memory boards.

Power-On Reset

The Power-On Clear circuit on the Altair 8800 and 8800a does not work properly, requiring you to toggle the Reset switch on the front panel of these machines after power-on. MITS fixed this on the Altair 8800b, by synchronizing its reset signal with the system clock. The 88-2SIOJP includes a synchronized Power-On Reset circuit that is similar to the Altair 8800b’s reset circuit. You can optionally connect this Power-On Reset circuit to the S-100 Reset signal for correct power-on reset operation.

CONFIGURATION

The 88-2SIOJP comes in two configurations that differ mainly in the kind of connectors used for the serial ports:

1. The M156 option has two 10-pin Molex-type 0.156” connectors that are compatible with the MITS 88-2SIO.
2. The R100 option has two 26-pin ribbon cable connectors that allow simple connection to DB25 connectors on the back of the Altair, using a straight-through (off-the-shelf) IDC ribbon cable assembly.

Both of these configurations provide the same functionality, though setup is a little different for the two. Find the appropriate section in this manual for your configuration.

It is also possible to configure one port of the 88-2SIOJP with the M156 option and the other with the R100 option.

88-2SIOJP M156 Configuration

The two 10-pin Molex connectors (S1 and S2) are connected as follows:

PIN	Function	Direction	Port 0 Jumpers	Port 1 Jumpers
1	RS-232 CTS	In	J2(1-2)	J3(1-2)
2	RS-232 DCD	In	J2(3-4), J11(2-3), Remove all J3	J3 (3-4), J13(2-3), Remove all J2
	-12V	Out	J11(1-2)	J13(1-2)
3	RS-232 RTS	Out	-	-
4	Ground	-	-	-
5	TTY +TxD	Out	-	-
6	TTY -RxD	In	-	-
7	RS-232 RxD	In	Remove J6	Remove J7
	TTL RxD	In	Remove J6	Remove J7
	TTY +RxD	In	J6(1-2)	J7(1-2)
8	RS-232 TxD	Out	-	-
9	TTL TxD	Out	J12(2-3)	J14 (2-3)
	+12V	Out	J12(1-2)	J14(1-2)
10	Ground	-	-	-

If DCD is provided for one port then neither DCD nor CTS is available for the other port. This is because DCD “borrows” the RS-232 line receiver from the CTS circuit of the other port.

RS-232 Communication with the M156 Option

For normal RS-232 connection, jumper either port as follows:

Jumper	Port 0	Port 1
J2	1-2*	
J3		1-2*
J6	Remove	
J7		Remove
J11	Remove	
J12	Remove	
J13		Remove
J14		Remove

* If handshaking is not required then J2 and/or J3 may be removed.

For a standard RS-232 connection, connect the 88-2SIOJP to the Altair rear panel with a wiring harness as follows:

Signal	Direction	88-2SIOJP S1 or S2 pin	DB25S pin
TxD	Out	8	3
RxD	In	7	2
CTS	Out	1	5
RTS	In	3	4
DCD*	In	2	20
GND		4 (or 10)	7

* If either port requires the DCD handshaking input signal, then it must borrow the other port's RTS line receiver:

Jumper	DCD on Port 0	DCD on Port 1
J2	3-4	Remove all
J3	Remove all	3-4
J11	2-3	Remove 2-3
J13	Remove 2-3	2-3

Handshaking inputs default to the "active" state if they are not connected. (Usually, only TxD, RxD and GND need to be connected.)

20 mA Current Loop Communication with the M156 Option

The 88-2SIOJP supports 20 mA current loop communication on both ports. For 20 mA communication, jumper either port as follows:

Jumper	Port 0	Port 1
J2	remove	
J3		remove
J6	1-2	
J7		1-2
J11	Remove	
J12	Remove	
J13		Remove
J14		Remove

For TTY connection, connect the 88-2SIOJP to the Altair rear panel, and the Altair to the Teletype with wiring harnesses as follows. (This is the same pinout as shown in the MITS 88-2SIO manual.)

Signal	88-2SIOJP S1 or S2 pin	DB25S pin	Teletype ASR33 Terminal Strip
+TxD	5	3	7
-TxD	4	2	6
+RxD	7	5	4
-RxD	6	4	3
Clip pin		1	

TTL Communication with the M156 Option

For TTL communication, jumper either port as follows:

Jumper	Port 0	Port 1
J2	remove	
J3		remove
J6	remove	
J7		remove
J11	Remove	
J12	2-3	
J13		remove
J14		2-3

For compatibility with the MITS 88-2SIO, connect the 88-2SIOJP to the Altair rear panel with a wiring harness as follows:

Signal	Direction	88-2SIOJP S1 or S2 pin	DB25S pin
TTL TxD	Out	9	3
TTL RxD	In	7	2
GND		4	7

External Device Power with the M156 Option

The 88-2SIOJP can provide up to about 500 mA of regulated +12V and -12V to a device connect to it port, at the expense of other (seldom used) functionality. +12V replaces the TTL output, and -12V replaces the DCD input, if you select these options, as follows:

Function	88-2SIOJP S1 or S2 pin	Jumper Port 0	Jumper Port 1
+12V	9	J12(1-2)	J14(1-2)
-12V	2	J11(1-2)	J13(1-2)

There is no standard for connecting +12V and -12V to the DB25 connector at the rear of the Altair, so feel free to use whichever unused pins suit your needs.

88-2SIOJP R100 Configuration

The pins of the two 26-pin ribbon cable connectors (S3 and S4) are assigned such that a straight-through ribbon cable to a DB25S connector will provide normal RS-232 connections, as follows:

88-2SIOJP S3 or S4 PIN	DB25S PIN	Function	Dir.	Port 0 Jumpers	Port 1 Jumpers
2	14	TTY -RxD	In	J4(1-2)	J8(1-2)
3	2	RS-232 RxD	In	Remove J6	Remove J7
		TTL RxD	In	Remove J6	Remove J7
		TTY +RxD	In	J6(1-2)	J7(1-2)
5	3	RS-232 TxD	Out	-	-
7	4	RS-232 CTS	In	J2(1-2)	J3(1-2)
9	5	RS-232 RTS	Out	-	-
12	19	TTY +TxD	Out	J5(1-2)	J9(1-2)
13	7	Ground	-	-	-
14	20	RS-232 DCD	In	J2(3-4), J11(2-3), Remove all J3	J3 (3-4), J13(2-3), Remove all J2
		-12V	Out	J11(1-2)	J13(1-2)
24	25	TTL TxD	Out	J12(2-3)	J14 (203)
		+12V	Out	J12(1-2)	J14(1-2)

Note that if DCD is provided for one port, then neither DCD nor CTS is available for the other port. This is because DCD “borrows” the RS-232 line receiver from the CTS circuit of the other port.

RS-232 Communication with the R100 Option

For normal RS-232 connection, jumper either port as follows:

Jumper	Port 0	Port 1
J2	1-2*	
J3		1-2*
J4	Remove	
J5	Remove	
J6	Remove	
J7		Remove
J8		Remove
J9		Remove
J11	Remove	
J12	Remove	
J13		Remove
J14		Remove

* If handshaking is not required then J2 and/or J3 may be removed.

Connect the 88-2SIOJP to the Altair rear panel with straight-through ribbon cable, producing the following RS-232 connections:

Signal	Direction	88-2SIOJP S3 or S4 pin	DB25S pin
TxD	Out	5	3
RxD	In	3	2
CTS	Out	7	5
RTS	In	9	4
DCD*	In	14	20
GND		13	7

* If either port requires the DCD handshaking input signal, then it must borrow the other port's RTS line receiver, as follows:

Jumper	DCD on Port 0	DCD on Port 1
J2	3-4	Remove all
J3	Remove all	3-4
J11	2-3	Remove 2-3
J13	Remove 2-3	2-3

Handshaking inputs default to the "active" state if they are not connected. (Usually, only TxD, RxD and GND need to be connected.)

20 mA Current Loop Communication with the R100 Option

The 88-2SIOJP supports 20 mA current loop communication on both ports. For 20 mA communication, jumper either port as follows:

Jumper	Port 0	Port 1
J2	remove	
J3		remove
J4	1-2	
J5	1-2	
J6	1-2	
J7		1-2
J8		1-2
J9		1-2
J11	Remove	
J12	Remove	
J13		Remove
J14		Remove

Connect the 88-2SIOJP to the Altair rear panel with a straight-through ribbon cable, and connect the Altair to the Teletype with a wiring harness as follows. (Other signals on the DB25 connector should be left unconnected. Note that the DB25 does not have the same pinout as shown in the MITS 88-2SIO manual.)

Signal	88-2SIOJP S3 or S4 pin	DB25S pin	Teletype ASR33 Terminal Strip
+TxD	12	19	7
-TxD	13	7	6
+RxD	3	2	4
-RxD	2	14	3

TTL Communication with the R100 Option

For TTL communication, jumper either port as follows:

Jumper	Port 0	Port 1
J2	remove	
J3		remove
J4	Remove	
J5	Remove	
J6	remove	
J7		remove
J8		remove
J9		remove
J11	Remove	
J12	2-3	
J13		remove
J14		2-3

Connect the 88-2SIOJP to the Altair rear panel with a straight-through ribbon cable, and connect as follows. (Other signals on the DB25 connector should be left unconnected.)

Signal	88-2SIOJP S3 or S4 pin	DB25S pin
TTL TxD	24	25
TTL RxD	3	2
GND	13	7

R100 External Device Power

The 88-2SIOJP can provide up to about 500 mA of regulated +12V and -12V to a device connect to it port, at the expense of other (seldom used) functionality. +12V replaces the TTL output, and -12V replaces the DCD input, if you select these options, as follows:

Function	88-2SIOJP S3 or S4 pin	DB25S Pin	Jumper Port 0	Jumper Port 1
+12V	24	25	J12(1-2)	J14(1-2)
-12V	14	20	J11(1-2)	J13(1-2)

Open Collector Control Output on Port 0

For applications that require an open-collector control output (such as for controlling the paper tape reader on certain Teletypes), Port 0’s RTS signal can be configured with an open-collector driver, rather than its normal RS-232 driver:

1. Cut trace between pins 1 and 2 of J10, in the solder side
2. Install 10K-ohm resistor in R11
3. Install 1n4148 diode in D1
4. Install 2N3904 transistor in Q1
5. Install jumper between pins 2 and 3 of J10

(This option can be disabled by simply moving the jumper to connect J10 pins 1 and 2 instead of 2 and 3.)

With this option installed, writing 11h to Port 0’s Control Port will turn on the open-collector driver (pulling the RTS pin to ground). Writing 51h to the Control Port will turn off the open-collector driver, allowing the RTS pin to float.

Baud Rate Selection

The baud rate can be set independently for each port. DIP Switch SW4 selects Port 0's baud rate, and DIP Switch SW5 sets Port 1's baud rate, as indicated on the PC board. (These baud rates assume that the 68B50 ACIAs are configured for ÷16 clocks. Additional baud rates can be achieved by configuring the ACIAs for ÷64 clocks.) Close the one switch that selects the desired baud rate for each port, and leave all other switches open.

DIP Switch SW4 Position	Baud Rate
1	76800
2	38400
3	19200
4	9600
5	4800
6	2400
7	1200
8	600
9	300
10	110

Interrupts

The 88-2SIOJP is designed to provide 8-level vectored interrupts, single-level interrupts, or no interrupts at all. Interrupts are configured by installing jumpers in a 16-pin DIP header that is installed in location J15.

If single-level interrupts are selected, then the interrupt routine in software must poll all devices with interrupt capability, to determine and resolve the source of the interrupt.

Vectored interrupts require a vectored interrupt controller (such as the MITS 88-VI-RTC board) to be installed in the Altair.

J15 pins are assigned as follows:

J15 Pin	Function	J15 Pin	Function
1	S-100 Interrupt Input	16	Vector 7
2	Port 0 Interrupt Output	15	Vector 6
3		14	Vector 5
4		13	Vector 4
5		12	Vector 3
6		11	Vector 2
7	Port 1 Interrupt Output	10	Vector 1
8	S-100 Interrupt Input	9	Vector 0

Connect pin 1 to pin 2 for single-level interrupts from Port 0.
Connect pin 7 to pin 8 for single-level interrupts from Port 1.

Connect pin 2 to one of the Vector pins for vectored interrupts from Port 0. Connect pin 7 to one of the Vector pins for vectored interrupts from Port 1.

I/O Port Address Selection

The two I/O Port ACIAs occupy four sequential I/O ports in the Altair. The first address is Port 0's control and status port; the second is Port 0's data port; the third is Port 1's control and status port; the fourth is Port 1's data port.

Positions 1 through 6 of DIP Switch SW2 set the serial port address, where a closed switch represents a binary 0, and an open switch represents a binary 1. Switch 6 is the highest-order bit, and switch 1 is the lowest.

Note that MITS software assumes the "terminal" (console) serial port occupies port addresses 10h and 11h (020 and 021 octal). To set the 88-2SIOJP for addresses 10h through 13h, set SW2 as follows:

DIP Switch SW2 Position	Address Bit	Setting
1	A2	Closed
2	A3	Closed
3	A4	Open
4	A5	Closed
5	A6	Closed
6	A7	Closed
7		-
8		-

EPROM Setup

EPROM Address and Enable

When enabled, the EPROM occupies 2K-bytes of memory space in the Altair. The starting address of the EPROM is set with positions 1 through 5 of DIP switch SW3, where a closed switch represents a binary 0, and an open switch represents a binary 1. Switch 5 is the highest-order bit, and switch 1 is the lowest. The firmware that ships standard with the 88-2SIOJP assumes this memory is the highest 2K block of memory (starting at address F800h), meaning that SW3 is set as follows:

DIP Switch SW3 Position	Address Bit	Setting
1	A11	Open
2	A12	Open
3	A13	Open
4	A14	Open
5	A15	Open
6		-
7		-
8		-

The EPROM may be disabled in two ways:

1. Opening SW2 position 7 (which is labeled “EE”) completely disables the EPROM
2. When enabled, the EPROM Auto-Disable circuit will disable the EPROM whenever an IN instruction from port FFh is executed.

EPROM Auto-Disable

Closing SW2 position 8 (which is labeled “ED”) enables the EPROM Auto-Disable feature.

If the EPROM Auto-Disable feature is enabled, then the EPROM is enabled whenever the Altair is reset, and becomes disabled when the Altair performs an IN instruction from the front panel switch register, I/O port address 377 octal (FFh).

EPROM Address Overlay

The EPROM can overlay other memory in the Altair, occupying the same address space as the other memory. While the EPROM is enabled (including by the Auto-disable circuit), the CPU will read from toe 88-2SIOJP’s EPROM instead of the other memory device, provided one of the two System Memory Disable switches is closed. See System Memory Disable section on the next page.

Jump-Start

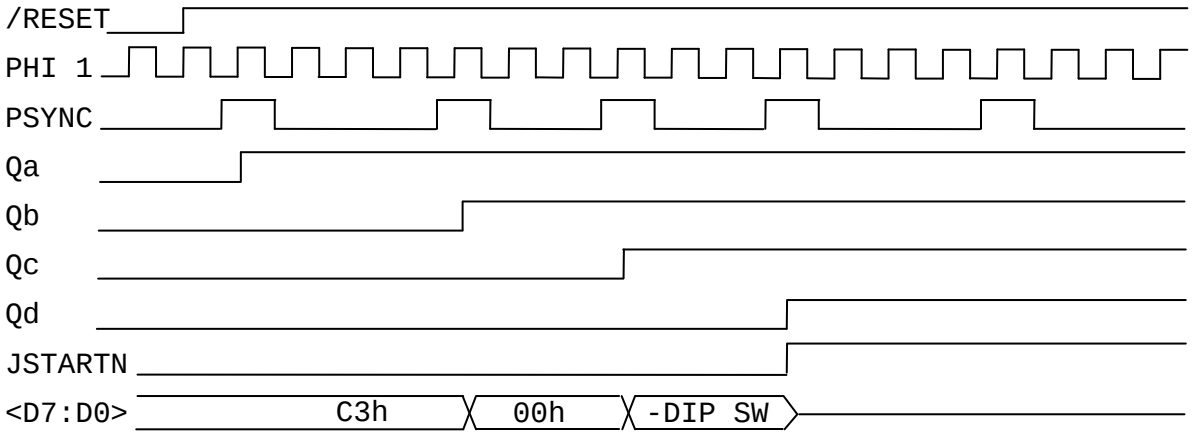
Jump-Start is enabled either by setting DIP Switch SW3 position 6 (which is labeled “JS”) to the ON position, and either position 7 (which is labeled “SD”) to the ON position or position 8 (which is labeled “PH”) to the ON position. See System Memory Disable section on the next page for details about the SD and PH switches.

When Jump-Start is enabled, the 88-2SIOJP will force a jump to the specified Jump-Start address when the Altair is reset. The high byte of the Jump-Start address is set with DIP Switch SW1, where a closed switch represents a binary 1, and an open switch represents a binary 0. (Note that this is the opposite of the other DIP switches.) Switch 8 is the highest-order bit, and switch 1 is the lowest. The low byte of the Jump-Start address is always 00h. For example, to set the Jump-Start address to the first address in the EPROM at its standard address of F800h, set SW1 as follows:

DIP Switch SW1 Position	Address Bit	Setting
1	A8	Open
2	A9	Open
3	A10	Open
4	A11	Closed
5	A12	Closed
6	A13	Closed
7	A14	Closed
8	A15	Closed

Jump-Start Theory of Operation

Jump-Start works by forcing a JMP instruction (C3h followed by two address bytes) onto the bus immediately following Reset. Shift register A (a 74LS195) is the state machine that sequences the three machine cycles required for this jump instruction as follows:



System Memory Disable

In order to perform Jump-Start, the 88-2SIOJP must disable other memory in the Altair starting at address 0000h, for three machine cycles while the JMP instruction is forced onto the bus. Also, in order to overlay the EPROM over other system memory, the 88-2SIOJP must disable other memory in the Altair that is at the same address as the EPROM whenever the EPROM is being accessed.

The 88-2SIOJP supports two methods of disabling other memory in the Altair. The first is by blocking the SMEMR signal on the S-100 bus when it needs to disable other memory. This method will work with most early S-100 memory boards, including all memory boards made by MITS. To select this method of disabling other memory, close DIP switch SW3, position 7 (which is labeled “SD”).

The other method of disabling system memory for Jump-Start and EPROM access is via the PHANTOM signal on the S-100 bus. PHANTOM is a newer S-100 signal, created after the Altair. Many S-100 boards, including many early ones, support the Phantom signal, though no MITS boards do. To select this method of disabling other memory, close DIP switch SW3, position 8 (which is labeled “PH”). Note that it is probably okay to have both position 7 and position 8 closed.

System Memory Disable Theory of Operation

Most S-100 memory boards, including all memory boards made by MITS, will drive their data onto the S-100 bus only when PDBIN is high and SMEMR is high. (SMEMR is used to distinguish between reads from memory and reads from I/O devices.) The 88-2SIOJP must prevent other memory boards from driving data onto the bus when it is performing the Jump-Start JMP instruction and when the CPU is accessing the 88-2SIOJP’s EPROM (which may overlay other memory in the system). One way to block

memory boards from driving data onto the S-100 bus is to block the SMEMR signal.

The 88-2SIOJP blocks the SMEMR signal on the S-100 bus by asserting the Status Disable signal, STSBn. While this signal is asserted, the Altair CPU does not drive any of the 8 status signals. (These signals are SINP, SOUT, SINTA, SMEMR, SWON, SHLTA, SSTACK, and SM1. Note that SMWRITE is not on this list, as it is generated by the Altair front panel.)

The 8802SIOJP generates its own version of these signals when it asserts STSBn, notably with SMEMR de-asserted. These status signals are driven as follows:

Signal	Level
SINP	Low (de-asserted)
SOUT	Low (de-asserted)
SINTA	Low (de-asserted)
SMEMR	Low (de-asserted)
SWON	High (de-asserted)
SHLTA	As generated by the CPU
SSTACK	As generated by the CPU
SM1	As generated by the CPU

The SHLTA, SSTACK, and SM1 signals are driven to their correct levels only so that the front panel display is correct during Jump-Start and EPROM access.

This method of disabling system memory is cumbersome, and so (sometime after the Altair was created), the PHANTOM signal was added to the S-100 bus. Many memory boards support PHANTOM by not driving data onto the S-100 bus when PHANTOM is low (asserted). The 88-2SIOJP also supports this mechanism, as described in the Configuration section.

Regardless of which method for disabling another RAM board in the system, only read operations are blocked for the other RAM board. Writes to the other RAM board will still write to its memory, while writing to EEPROM on the 88-2SIOJP.

Note that the MITS 8800b Turnkey Module performs Jump-Start by overriding the SMEMR signal on the S-100 bus, using (on earlier versions of the board) a big transistor, or (on later versions of the board) six open-collector buffer elements in parallel. Overdriving a TTL signal in this way is a questionable design practice.

Power-On Reset

The 88-2SIOJP’s Power-On Reset circuit can reset the Altair correctly at power-on.

Power-On Reset Setup

If you are installing the 88-2SIOJP in an Altair 8800 or 8800a, then you can jumper pins 1 to pin 2 on J16 to connect the 88-2SIOJP’s onboard CPU-synchronized power-on clear circuit to the S-100 Reset

signal, thereby eliminating the need to toggle the Altair's Reset switch after power-on.

The Power-On Clear and reset circuits of the Altair 8800b work correctly, and only need to be connected together. For installation in an Altair 8800b, you can jumper pins 2 to 3 on J16 to connect the Altair's own Power-On Clear circuit to its Reset signal, eliminating the need to toggle the Altair's Reset switch after power-on. (This connection is made in the small front panel board of the Altair 8800bt - the Turnkey version.)

Modifying an Altair to Run at Power-On

The Run/Stop flip-flop in the front panel of the Altair 8800 and 8800a is not set or cleared at power-on, and so will be in a random state after power-on. If it happens to be in the Stop state, then you will still need to toggle the Run switch. A simple, non-destructive modification to the Altair front panel will initialize this flip-flop at power-on to the Run state: Install the following four jumper wires on the Altair front front panel's PC board:

1. Jumper IC H pin 9 to IC E pin 4
2. Jumper IC E pin 3 to IC R pin 10
3. Jumper IC R pin 9 to IC J pin 6
4. Jumper IC R pin 8 to IC R pin 7.

The Run/Stop flip-flop of the Altair 8800b is initialized to the Stop state at power-on. Modifying an Altair 8800b to run at power-on requires more extensive modifications, including cutting some traces.

Power-On Reset Theory of Operation

In all versions of the Altair 8800, the CPU board generates a Power-On Clear signal that just drives a signal on the S-100 bus - it does not cause a CPU reset on power-on. Only the Altair 8800bt connects the Power-On Clear signal to the Reset signal, causing a Power-On Reset.

The Intel 8080A specification does not provide complete requirements for the 8080A Reset signal. As a result, the Power-On Clear signal in the Altair 8800 and 8800a does not work correctly: if you connect this signal to the Altair's Reset signal, the CPU will not reset reliably.

Intel addressed this problem by synchronizing the reset signal in the 8080 companion chip, the 8224 Clock Generator. The Altair 8800b family uses this chip, making Power-On Reset possible in these machines.

The 88-2SIOJP includes an improved Power-On Clear circuit that senses the power supply voltage, and begins a clear pulse after the power supply has reached operating voltage. This clear signal is then synchronized with the 8080A's Phi-2 clock, in the same way the 8224 synchronizes Reset. You can connect this Power-On Clear signal (with a jumper) to the Reset signal, to provide a reliable Power-On Reset to the Altair.

USING THE SERIAL PORTS

The 88-2SIOJP's two serial ports are based on the Motorola MC68B50 ACIA, and are designed to be compatible with the MITS 88-2SIO. See the Motorola MC6850 data sheet (DS9493R4, © 1995 Motorola) for details.

The base I/O address of the ACIAs is set by a DIP switch, as explained in the previous section. The 8802SIOJP occupies four sequential I/O addresses, starting at this base address. The first two addresses are the control and data ports for Port 0; the second two are the control and data ports for Port 1:

Address		Port #	Output Function	Input Function
A1	A0			
0	0	0	Control Register	Status Register
0	1	0	Transmit Data Register	Receive Data Register
1	0	1	Control Register	Status Register
1	1	1	Transmit Data Register	Receive Data Register

Data Registers

Data can be written to one of the Transmit Data Registers whenever the TDRE bit in the corresponding Status Register is high. Writing to the Transmit Data Register will clear that TDRE bit, which will remain clear until the ACIA transfers the data to its Transmit Shift Register for serialization.

The RDRF bit in one of the Status Registers will become high when the corresponding ACIA transfers a complete data word from its Receive Shift Register to its Receive Data Register, and will remain high until software reads from that Receive Data Register.

Control Registers

Each Port has an 8-bit control register that allows port configuration under software control. Each bit is defined as follows. (All bits are active-high.)

7	6	5	4	3	2	1	0
Input Interrupt	Output Interrupt		Transmission Bits			Clock Divide & Reset	

Bits 1 and 0 of each Control Register control the clock divider and master reset as follows:

Bit 1	Bit 0	Function
0	0	÷ by 1 clock
0	1	÷ by 16 clock
1	0	÷ by 64 clock
1	1	Master Reset

Software should first issue a Master Reset command to each serial port, by setting bits 1 and 0 of each control port to 1. For normal operation, the divide by 16 clock rate is then selected, by setting

bits 1 and 0 to 01b. Other (lower) baud rates are possible by selecting the divide by 64 clock rate - in which case the baud rate will be 1/4 of the baud rate printed on the PC board silkscreen.

Bits 4, 3, and 2 of each Control Register set the word length, parity, and number of stop bits:

Data Bit			Function		
4	**3**	**2**	**# of Data Bits**	**# of Stop Bits**	**Parity**
0	0	0	7	2	Even
0	0	1	7	2	Odd
0	1	0	7	1	Even
0	1	1	7	1	Odd
1	0	0	8	2	None
1	0	1	8	1	None
1	1	0	8	1	Even
1	1	1	8	1	Odd

Bits 7, 6, and 5 of each Control Register control interrupts and handshaking:

Data Bit			Function
7	**6**	**5**	
X	0	0	RTS active, transmit interrupt disabled
X	0	1	RTS active, transmit interrupt enabled
X	1	0	RTS inactive, transmit interrupt disabled
X	1	1	RTS inactive, transmit interrupt disabled, transmits a BREAK on the transmit data line
0	X	X	Receive interrupt disabled
1	X	X	Receive interrupt enabled

The following 8080 code example illustrates initializing Port 0’s ACIA (at its standard I/O address) for 8 data bits and 2 stop bits:

```
3E 03   MVI   A,ARESET     ;Reset command
D3 10   OUT   CONTROL0     ;...to the control port
3E 71   MVI   A,ASETUP     ;8 data bits, 2 stop bits,
                           ;RTS active, interrupts enabled
D3 10   OUT   CONTROL0     ;..to the control port
```

Status Registers

Each status register provides 8 status bits for the respective Port, as follows:

Bit	Name	Function
7	IRQ	Interrupt Request
6	PE	Parity Error
5	OVRN	Overrun Error
4	FE	Framing Error
3	-CTS	Clear to Send (active low)
2	-DCD	Data Carrier Detect (active low)
1	TDRE	Transmit Data Register Empty
0	RDRF	Receive Data Register Full

The IRQ bit will be high whenever the ACIA is requesting an interrupt. If transmit interrupt interrupts are enabled, then it will be high if the transmit data register is empty (and therefore the TRDE bit is high). If receive interrupts are enabled, then the IRQ bit will be high if the receive data register is full (and therefore the RDRF bit is high).

The three error conditions (PE, OVRN and FE) apply to the currently-received data in the receive data register, and are valid while the RDRF bit is high.

The -CTS bit will be low whenever the RS-232 CTS signal is true, indicating that the ACIA may transmit data. When this bit is high, the RS-232 signal is false, and data transmission is inhibited by hardware within the ACIA.

The -DCD bit will be low whenever the RS-232 DCD signal is true, indicating that the ACIA may receive data. When this bit is high, the DCD signal is false, and data reception is inhibited by hardware within the ACIA.

A 0-to-1 transition of the -DCD bit generates an interrupt if the receive interrupt is enabled. This interrupt is cleared by first reading the Status Register, and then reading the Data Register, or by issuing a Master Reset command.

The TDRE and RDRF bits are discussed in the Data Registers section above.

USING THE EPROM/EEPROM

The EPROM socket supports both a 2716-type EPROM and many of the 2816-type EEPROMs. The 88-2SIOJP always inserts one wait state when reading from the EPROM or EEPROM, and so the minimum required access time is greater than 600 uS.

When using an EPROM, J1 should be jumpered from pin 1 to pin 2 always.

When using an EEPROM, J1 should be jumpered from pin 1 to pin 2 normally, to prevent accidental writing. (Note that many programs will

write to memory and then read it back, to determine if RAM is available at a given location, for example when testing to see how much RAM is in the system. Such a write could destroy saved data in an EEPROM if writing is enabled.)

Jumpering J1 from pins 2 to 3 enables writing to the EEPROM. Several 2816 EEPROM types exist, differing mainly in their write algorithms. The following chart illustrates most of the types of 2816's, and indicates which of them can be written to by the 88-2SIOJP.

Manufacturer	Part #	88-SIOJP Support	Write Completion Method
Atmel	28C16	Yes	Polled
Atmel	28C16E	Yes	Polled
Catalyst	CAT28C16A	Yes	Polled
Exel	EX2816A	Yes	Polled
Exel	EX28C16A	Yes	Polled
Intel	2815	No	21V Vpp
Intel	2816	No	21V Vpp
Intel	2816A	No	Long Write Pulse
Microchip	28C16A	Yes	Polled
Samsung	KM2816A	Yes	Timed
On Semiconductor	CAT28C16A	Yes	Polled
Seeq	2816A	Yes	Timed
Seeq	52B13	No	Long Write Pulse
Seeq	5516A	Yes	Timed
Xicor	X2816B	Yes	Polled

The 88-2SIOJP does not support EEPROMs that require special Vpp programming voltages nor EEPROMs that require long write pulses. These EEPROMs may still be used for read-only on the 88-2SIOJP (and treated exactly like 2716 EPROMs), but they must be programmed elsewhere.

Writing to the EEPROM must be done via a program; it cannot be done from the front panel.

Note that writing to the EEPROM will also write to any other RAM board on the S-100 bus that shares its memory address with the 88-2SIOJP. The System Memory Disable function that allows the 8-2SIOJP's EEPROM to overlay other RAM does not block write operations on the S-100 bus.

Polled EEPROM Write Completion

EEPROMs with polled write completion will output data with data bit 7 inverted until the write has completed. Software should test for write completion after each byte is written, as follows:

```
;HL points to the EEPROM address to be written
;B = the data to write
EEWRITE:  MOV   M,B       ;Write to EEPROM
          LXI   D,1860d   ;Set 40 mS timeout timer (decimal value)

LOOP:     DCX   D         ;Bump timeout timer
```

```
            MOV   A,D       ;Test for timeout
            ORA   E
            JZ    ERROR

            MOV   A,M       ;Read back from EEPROM
            CMP   B         ;Done?
            JNZ   LOOP      ;n: keep waiting

            RET             ;Successful write
```

Timed EEPROM Write Completion

Timed write completion requires software to wait at least 10 mS after writing to the EEPROM, before accessing the EEPROM again:

```
     ;HL points to the EEPROM address to be written
     ;B = the data to write
     EEWRITE:  MOV   M,B       ;Write to EEPROM
               LXI   D,917d    ;Set up 11 mS timer (decimal value)

     LOOP:     DCX   D         ;Bump completion timer
               MOV   A,D       ;Test for completion
               ORA   E
               JNZ   LOOP

               RET
```

EXTENDER BOARDS IN EARLY ALTAIRS

The original Altair 8800 came with a 4-slot backplane. If you wanted more than 4 slots, then additional 4-slot backplanes could be added, connecting to each other via 100 short pieces of wire. Later Altairs (including the Altair 8800a and 8800b, as well as some 8800’s) came with an 18-slot backplane.

If your Altair has the original 4-slot backplane with additional backplane sections added, then testing the 88-2SIOJP (or for that matter, any S-100 board) on an S-100 extender board will probably not work reliably. This is because the S-100 signal quality is already compromised by the 100 jumper wires that connect the bus sections together. The additional signal degradation caused by the extender board will cause some signals to be too far out of spec to work correctly.

SPECIFICATIONS

General

Bus Compatibility:	Early S-100 machines including MITS Altairs, IMSAI 8080, Processor Technology Sol-20, Polymorphic Systems Poly-88. Not IEEE-696 compliant.
Max CPU speed:	2.2 MHz

PC Board

Material:	FR-4 material, green solder-mask over bare copper
Thickness:	0.062” +/- 0.006”
Traces:	15 mil minimum width, 1-oz copper
Silkscreen:	White, component-side only
Layers:	2
Edge Connector:	100-pin, electroless nickel immersion gold plating, 15° bevel

Serial Ports

Serial ports:	2
UART Type:	MC68B50
Baud Rates:	110, 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 76800 (DIP switch selectable)
Protocol:	RS232, 20 mA current loop (TTY), TTL
Handshaking:	RS-232 CTS, RTS, DCD Open-Collector RTS on Port 0 only
Aux Power Out:	Regulated +/-12V, 500 mA each
Wait States:	0
Connectors:	10-pin MOLEX (M156 option for compatibility) or 26-pin header (M100 option for straight-through ribbon cable to DB25)
Compatibility:	MITS 88-2SIO, MITS 8800b Turnkey Module

EPROM

EPROM/EEPROM Type:	2716 EPROM/single-voltage 2816A EEPROM
Max access time:	400 nS
Wait states:	0
Auto-disable:	Optional EPROM disabled on IN instruction from port FFh (Compatible with MITS software and 8800b Turnkey Module.)

Jump-Start

Jump-Start address:	DIP switch selectable to 256-byte page boundary
Compatibility:	* Status Disable compatible with early S-100 memory boards, including those made by MITS * Phantom compatible with most early memory boards that support Phantom

Power-On Clear

Trigger:	POC is triggered whenever Vcc falls below ~4.6V
Synchronization:	Positive edge of Phi-2 (Same as Intel 8224)

BILL OF MATERIALS

Component	Value	Reference Name	M156 Qty	R100 Qty
PC Board, 88-2SIOJP, Rev C			1	1
Diode, Signal	1N4148	D1-D5	5	5
Diode, 3.9V Zener	1N4730	D6	1	1
Resistor, 1/4W	220 Ohm	R5,R10,R12,R15,R18	5	5
Resistor, 1/4W	330 Ohm	R22,R23	2	2
Resistor, 1/4W	470 Ohm	R21	1	1
Resistor, 1/4W	1.5K Ohm	R6,R7,R16,R17	4	4
Resistor, 1/4W	2.7K Ohm	R13, R14,R20	3	3
Resistor, 1/4W	10K Ohm	R1-R4,R8,R9,R11,R19	8	8
Resistor, 1/4W	1K Ohm	R24 (Rework on Rev C)	1	1
14-pin DIP socket, 0.3" wide		B,F,G,J,K,L,M,P,Q,R,S,T,U,V,W,Y,FF	17	17
16-pin DIP socket, 0.3" wide		A,H,I,N,X,X,Z,AA,BB,CC,DD,EE,J14	13	13
24-pin DIP socket, 0.6" wide		D,E,F	3	3
R-pack, 10-Pin, 9-Resistor	2.2K Ohm	RP1-RP3	3	3
DIP Switch, 8-Position		SW1-SW3	3	3
DIP Switch, 10-Position		SW4,SW5	2	2
Crystal	4.9152 MHz	CR1	1	1
Capacitor, Electrolytic, 35V, Axial	10 uF	C9,C10,C21,C39,C40	5	5
Capacitor, Disk	0.1 uF	C1-C8,C11-C20,C22-C35,C37,C38	34	34
Capacitor, Disk	120 pF	C36	1	1
Header, 0.1", 2-pin		J6,J7	2	2
Header, 0.1", 2-pin		J4,J5,J8,J9	0	4
Header, 0.1", 3-pin		J1,J11-J14, J16	6	6
Header, 0.1", 4-pin		J2,J3	2	2
Shunt, 0.1", 2-Pin		J1,J16	2	2
Transistor, PNP	2N2907	Q2,Q3	2	2
Transistor, NPN	2N3904	Q1,Q4-Q6	4	4
Regulator, TO-220, +12V	7812	V3	1	1
Regulator, TO-220, -12V	7912	V2	1	1
Regulator, TO-220, +5V	7805	V1	1	1
Heat Sink, TO-220		V1	1	1
Machine Screw	4-40, 1/2"	V1-V3	3	3
Nut	4-40	V1-V3	3	3
Connector, Molex 0.156", 10-pin		S1,S2	2	0
Connector, Ribbon cable, 26-pin		S3,S4	0	2
IC, DIP, Quad 2-Input NAND Gate	74LS00	M,W,FF	3	3
IC, DIP, Hex Inverter	74LS04	J,Y	2	2

Component	Value	Reference Name	M156 Qty	R100 Qty
IC, DIP, Hex Open-Collector Buffer	74LS07	S	1	1
IC, DIP, Triple 3-Input NAND gate	74LS10	K	1	1
IC, DIP, Hex Schmitt Inverter	74LS14	V	1	1
IC, DIP, Triple 3-Input NOR gate	74LS27	U	1	1
IC, DIP, 8-Input NAND Gate	74LS30	B	1	1
IC, DIP, Dual D Flip-Flop	74LS74	L,R	2	2
IC, DIP, 4-bit Magnitude Comparator	74LS85	N,O	2	2
IC, DIP, Quad Exclusive-Or Gate	74LS86	T	1	1
IC, DIP, 4-Bit Loadable Counter	74LS161	EE	1	1
IC, DIP, Hex D Flip-Flip with Clear	74LS175	CC	1	1
IC, DIP, Quad Loadable Shift Register	74LS195	A	1	1
IC, DIP, Quad 2-1 Inverting MUX	74LS258	H,I	2	2
IC, DIP, Hex Tristate Buffer	74LS367	X,Z,AA,BB,DD	5	5
IC, DIP, 4-Bit Ripple Counter	74LS393	Q,P	2	2
IC, DIP, Quad RS232 Line Driver	1488	G	1	1
IC, DIP, Quad RS232 Line Receiver	1489	F	1	1
IC, DIP, EPROM, 2Kx8, Programmed with Amon Firmware	2716A	C	1	1
IC, DIP, ACIA (Asynchronous Communication Interface Adapter)	MC68B50	D,E	2	2

DRAWINGS

Baud Rate Generator

330 R22 — FFa 74LS00 — C38 0.1uF — 330 R23 — FFc 74LS00 — X1 4.9152 MHz — C36 120 pF — FFd 74LS00

Qa 74LS393 — Qb 74LS393 — SW4 (B76800, B38400, B19200, B9600, B4800, B2400, B1200, B600, B300, B110)

Pb 74LS393 — SW5

EE 74LS161 — FFb 74LS00 — Divide by 11

PU2

Serial Port 0

Serial Port 1

D 6850 — E 6850

R4 10K — R1 10K — R3 10K — R2 10K — J2 — J3

RXD0 CTSN0 TXD0 RTSN0 RXD1 CTSN1 TXD1 RTSN1

Interrupt Vector Selection Jumpers

J15 — R16 1.5K — Sc 74LS07

VI7n VI6n VI5n VI4n VI3n VI2n VI1n VI0n PINTn

UARTE SOUTN USELN

ADDRESS

A1N A0 A1 A0

EPROM/EEPROM

C 2716

J1 — 1-2 for EPROM, 2-3 for EEPROM Write Enable

ESELN MEMRN PWRN ISTSBN STATLAT RESETN S100OEN JSTARTN

Status Latch

Lb — DDb 74LS367 — DDa 74LS367 — DDc 74LS367 — DDf 74LS367 — DDe 74LS367 — DDd 74LS367 — BBe 74LS367 — BBf 74LS367

CC 74LS175

Sb 74LS07

STSBn sINP SINP sINTA sMEMR SWOn SWON sHLTA sSTACK sM1 sOUT SOUT LMEMR STARTN

Jumpstart Circuit

A 74LS195 — H 74LS258 — I 74LS258 — RP1 — SW1 — Vcc connection to RP1 via rework

PU4

BBd 74LS367 — BBa 74LS367 — AAc 74LS367 — AAb 74LS367 — AAa 74LS367 — AAd 74LS367 — BBb 74LS367 — BBc 74LS367

DI0 DI1 DI2 DI3 DI4 DI5 DI6 DI7

JCLK

S100INN — DATA

Zc 74LS367 — Zb 74LS367 — Zd 74LS367 — Zf 74LS367 — Za 74LS367 — Ze 74LS367 — AAe 74LS367 — AAf 74LS367

DO0 DO1 DO2 DO3 DO4 DO5 DO6 DO7

Spare Gates

Pa

Project: 88-2SIOJP	Engineer: M. Eberhard		
Sheet Title: Data Paths	Filename:		
Revision: C (reworked to C.1)	Date: 16 August 2016	Sheet: 1 of 3	Martin Eberhard

ADDRESS

Voltage Regulators

+8V 1 — UNREG8V — V1 7805 — C9 10 uF — C10 10 uF — C1 0.1 … C19 0.1 — C20 0.1 … C37 0.1 — Vcc
+8V 51
GND 100
GND 50
GND

-16V 52 — UNREG16VM — V2 7912 — -12V — C39 10 uF — C6 0.1 — GND
+16V 2 — UNREG16VP — V3 7812 — +12V — C40 10 uF — C8 0.1 — GND

Serial Port Address Decode

ACIA Port Address

Closed=EPROM enabled
Closed=Autodisable EPROM

SW2 — RP2 — PU1 — Vcc

N 74LS85 — A5 A4 A3 A2 — A0 A1 A2 A3 — B0 B1 B2 B3 — IA<B IA=B IA>B OA>B OA=B OA<B — GND

A6 — Va 74LS14 — A7N — Ta 74LS86 — Tb 74LS86 — Kc 74LS10

EPROM Disable on IN from FF

B 74LS30 — A5 A4 A3 A2 A1 A0 A6 A7

Ua 74LS27 — Wd 74LS00 — La 74LS74 (Pn D Cn Qn O) — USELN

EPROM Address Decode

SW3 — RP3 — PU2 — EPROM Address

closed=Jumpstart enabled
closed=Disable RAM via Status
closed=Disable RAM via Phantom

O 74LS85 — A15 A14 A13 A12 A11 — Jb 74LS04 — Td 74LS86 — Kb 74LS10

JSTARTN

Rework

Vf 74LS14 — Sa 74LS07 — R24 1K

Power-On Clear

D6 1N4730 3.9V — R17 1.5K — R19 10K — Q6 2N3904 — Q4 2N3904 — Q5 2N3904 — R18 220 — C21 10 uF — R20 2.7K — Vb 74LS14 — PU4 — Rb 74LS74 — Sf 74LS07 — J16

RESETn 75 — POCn 99 — Se 74LS07

Address Buffers

A1 80 — A0 79 — A2 81 — A3 31 — A4 30 — A5 29 — A6 82 — A7 83 — A8 84 — A9 34 — A10 37 — A11 87 — A12 33 — A13 85 — A14 86 — A15 32

Xb 74LS367 — Xe 74LS367 — Xd 74LS367 — Xa 74LS367 — Xc 74LS367 — Xf 74LS367 — Yd 74LS04 — A7N

Je 74LS04 — A1N — A1
Ja 74LS04 — A7N — A7

SINP 13 — Yf 74LS04
SOUT 11 — Ye 74LS04

Control Signals

PHI2 24
STARTN
MWRT 68
pWRn 77 — Tc 74LS86
LMEMR
pDBIN 78 — Yc 74LS04
SWON
pSYNC 76 — Ve 74LS14
PHI1 25 — Vd 74LS14 — R21 470
PU1

Ub 74LS27 — Vc 74LS14 — Mc 74LS00 — Jf 74LS04 — Md 74LS00 — Yb 74LS04 — Wc 74LS00 — Wb 74LS00 — Wb 74LS00 — Uc 74LS27 — Ka 74LS10

Sd 74LS07 — Ma 74LS00 — Mb 74LS00

Spare Gates

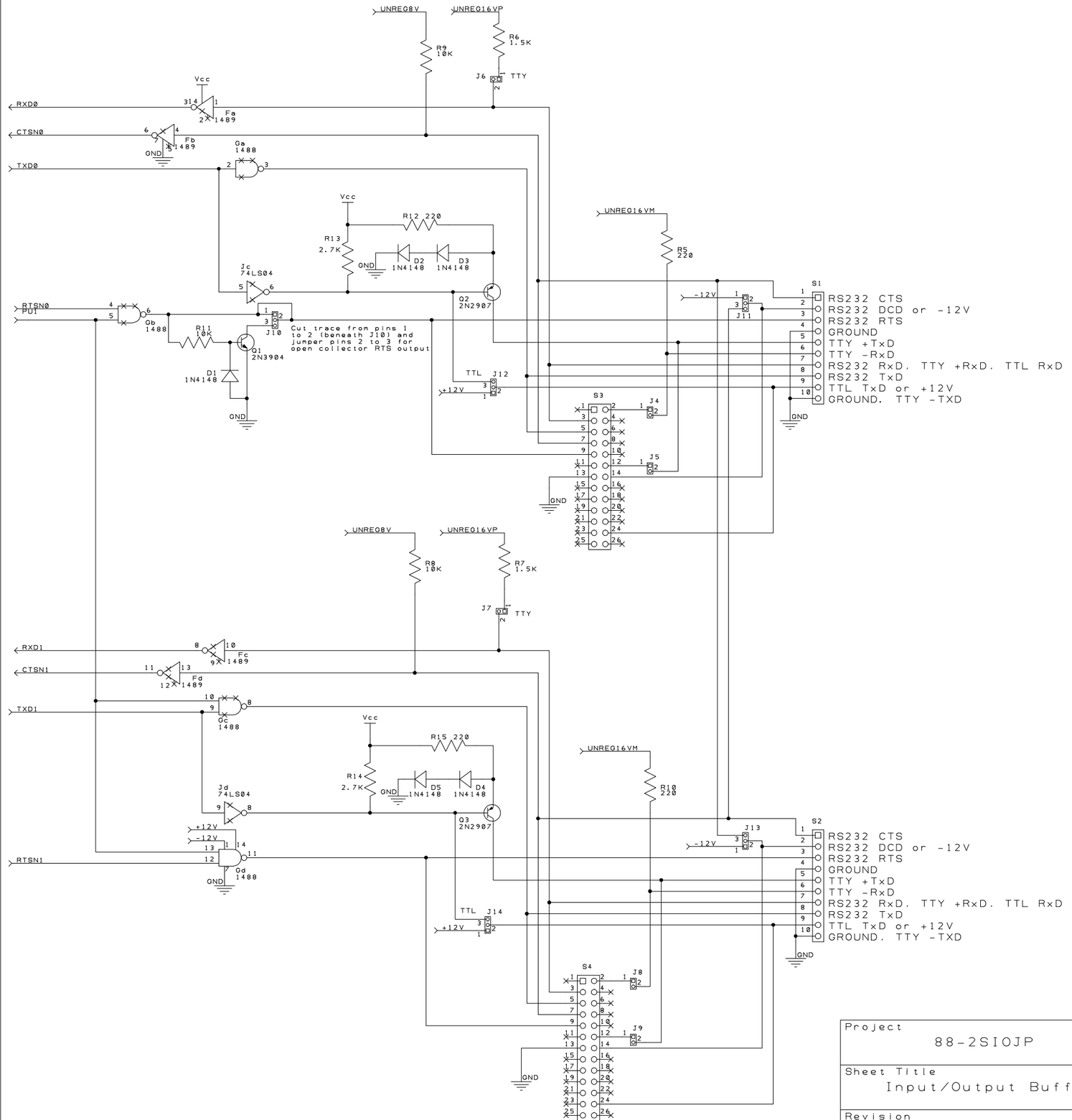
Ra 74LS74 (Pn D Cn Qn O)

Outputs

USELN
SOUTN
ESELN
RESETN
JSTARTN
ISTSBN
67 PHANTOMn
S100OEN
PDBINN
PWRN
UARTE
MEMRN
S100INN
STATLAT
JCLK

Project: 88-2SIOJP	Engineer: M. Eberhard	
Sheet Title: Control	Filename:	
Revision: C (reworked to C.1)	Date: 16 August 2016	Sheet: 2 of 3

Martin Eberhard



Port 0 Molex 156 Option:
Delete S3, J4, J5
Install TE Connectivity P/N 1-640-385-0 at S1

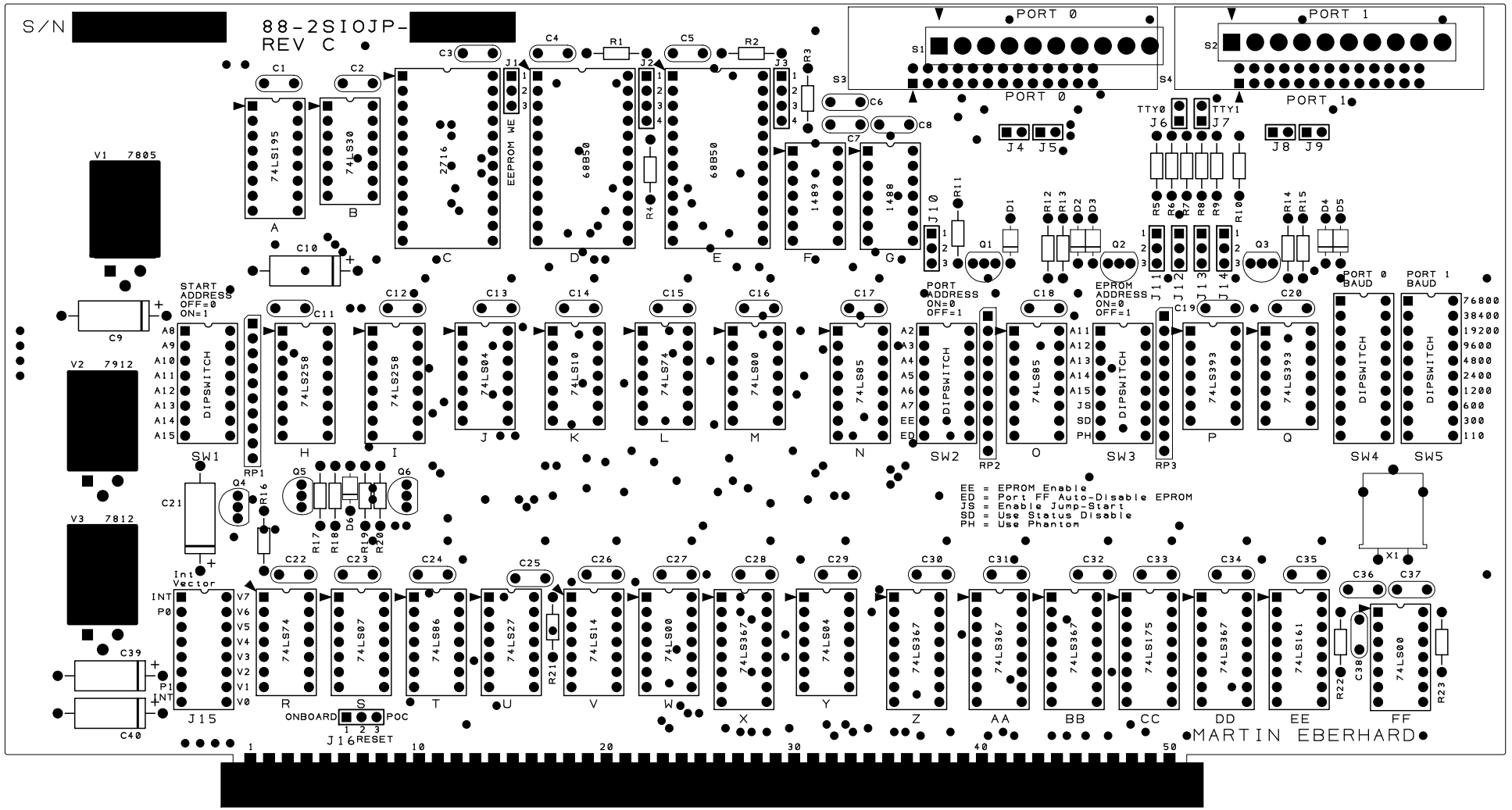
Port 0 Ribbon Cable Option:
Delete S1
Install TE Connectivity P/N 2-5499141-6 at S3
Install TE Connectivity P/N 87224-2 at J4, J5

Port 1 Molex 156 Option:
Delete S4, J8, J9
Install TE Connectivity P/N 1-640-385-0 at S3

Port 1 Ribbon Cable Option:
Delete S3
Installl TE Connectivity P/N 2-5499141-6 at S4
Install TE Connectivity P/N 87224-2 at J8, J9

Project: 88-2SIOJP	Engineer: M. Eberhard	
Sheet Title: Input/Output Buffers	Filename:	
Revision: C (reworked to C.1)	Date: 16 August 2016	Sheet: 3 of 3

Martin Eberhard


S/N [redacted]
88-2SIOJP-[redacted]
REV C
PORT 0
PORT 1
EEPROM WE
START ADDRESS OFF=0 ON=1
PORT ADDRESS ON=0 OFF=1
EPROM ADDRESS ON=0 OFF=1
PORT 0 BAUD
PORT 1 BAUD
TTY0
TTY1
EE = EPROM Enable
ED = Port FF Auto-Disable EPROM
JS = Enable Jump-Start
SD = Use Status Disable
PH = Use Phantom
Int Vector
ONBOARD
POC
RESET
MARTIN EBERHARD