IMSAI MFG. CORP. USER MANUAL

IMSAI® SYSTEM

FLOPPY DISK SYSTEM USER MANUAL

IMSAI®

OTHER IMSAI® PRODUCTS

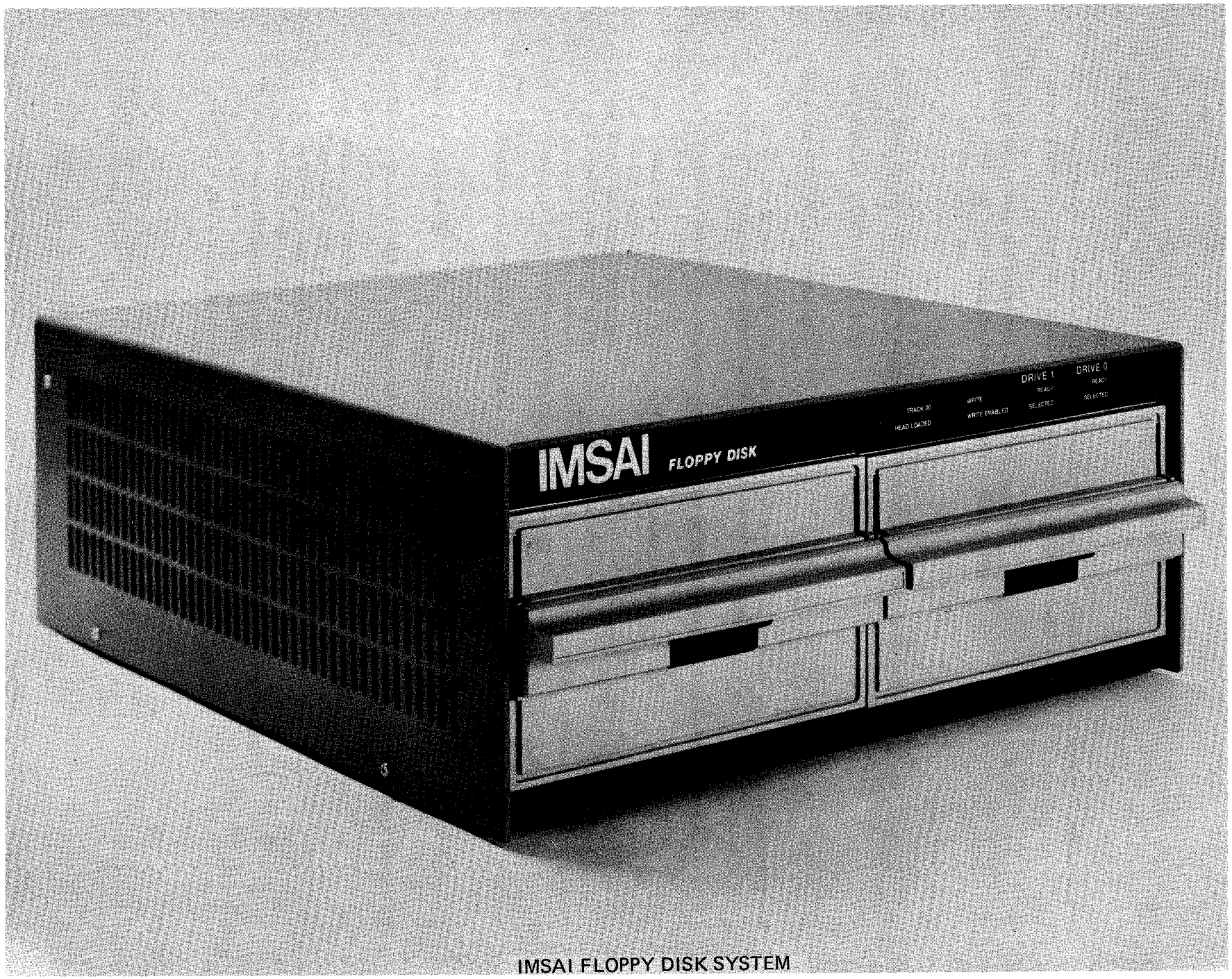
8080 MICROCOMPUTER SYSTEM
FLOPPY DISK SYSTEM
DISK OPERATING SYSTEM
LINE PRINTER SYSTEM
MULTIPROCESSOR SYSTEM
INTELLIGENT BREADBOARD SYSTEM
AP-44 MINI-PRINTER
HIGH-LEVEL LANGUAGES
8080 SYSTEM SOFTWARE
PTR-30 CHARACTER PRINTER SYSTEM
CRT TERMINAL SYSTEM
COMPLETE LINE OF S-100 CARDS

IMSAI
14860 WICKS BLVD.
SAN LEANDRO, CA.

CAUTION

FAILURE TO OBSERVE THESE IMPORTANT PRECAUTIONS WILL VOID WARRANTY

1. Read all material before beginning construction.
2. Use ONLY electronic quality rosin core solder.
3. Use extreme care with static-sensitive chips to prevent static discharge damage. (These chips are inserted in black conductive foam material in your kit.)
4. Do NOT plug or unplug boards while power is on.
5. Do NOT apply power to any board or circuit before checking each component and each trace.
6. Do NOT insert chips in socket before all soldering on the board is completed.
7. Do NOT use nonstandard parts such as fuses of a higher current rating.
8. Do NOT leave out any construction step.
9. Use only specified AC power.
10. Prevent flat cable end from touching areas of the system that may be carrying current.
11. Clean unit with soap and water or isopropyl alcohol only to prevent damage to plastic components.
12. Some repair operations are quite demanding. Do not attempt repairs beyond your level of skill to prevent damage to the board or the components.
13. Use ONLY a 25 watt electronic soldering iron for assembly of your IMSAI kit.
14. Do NOT perform any solder work on a board while power is applied.
15. Do NOT plug or unplug a chip from a socket while power is applied.
16. Check power supply voltages BEFORE inserting any boards into chassis.
17. For all assembled units, read USER GUIDE section for jumpering instructions.
18. To register your kit for warranty protection, fill out warranty cards and mail to IMSAI. Kits without warranty cards on file are NOT covered by warranty.



IMSAI FLOPPY DISK SYSTEM

IMSAI

FLOPPY DISK SYSTEM

Errata
4/7/77

IMPORTANT NOTICE

A Floppy Drive with Floppy Power Supply Rev. 3 is not compatible with a drive with FPS Rev.'s 0, 1 and 2; i.e., a dual drive system will not operate with a FPS Rev. 3 and one of the others. FPS Rev.'s 0, 1 and 2 are compatible, however. The difference is that with FPS Rev. 2 or earlier each drive requires a PLO Card, and with FPS Rev. 3 one PLO card is used for up to 4 drives. If you have recently purchased a drive with FPS Rev. 3 to modify a single drive system to dual, first check the Rev. # on the power supply in your present system. If it isn't Rev. 3, please notify one of our salespeople at 415-483-2093 before installing the new drive.

IMSAI FLOPPY DISK SYSTEM MANUAL

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IMSAI FLOPPY DISK SYSTEM MANUAL

TABLE OF CONTENTS

PURPOSE.....The IMSAI FLOPPY DISK MANUAL was designed as an aid and reference source to be used in understanding, assembling, and using the IMSAI FLOPPY DISK SYSTEM.

SCOPE.....It is assumed that the User is familiar with the operation of the IMSAI 8080 MICROCOMPUTER SYSTEM. Recommended references:

1. IMSAI 8080 USER MANUAL
2. INTEL 8080 Microcomputer Systems User Manual
3. Introduction To Microprocessors - Osborne and Associates

ORGANIZATION.....The IMSAI FLOPPY DISK MANUAL is organized into two major sections:

1. THE SYSTEM
2. COMPONENTS OF THE SYSTEM

THE SYSTEM section covers the operation of the IMSAI FLOPPY DISK as a SYSTEM.

THE COMPONENTS OF THE SYSTEM section covers the operation of the individual components which make up the IMSAI FLOPPY DISK SYSTEM.

WHAT TO DO WHEN YOU GET YOUR SYSTEM---------

* If you ordered an assembled FIF and FDC, proceed as follows:

  a. Turn to SYSTEM CONFIGURATION AND TESTING (p. 1 - 19).

* If you ordered and FIF kit and an assembled FDC, proceed as follows:

  a. Assemble the IFM as per the IFM ASSEMBLY INSTRUCTIONS (p. 2 - 17).

  b. Assemble the FIB as per the FIB ASSEMBLY INSTRUCTIONS (p. 3 - 23).

  c. Turn to SYSTEM CONFIGURATION AND TESTING (p. 1 - 19).

* If you ordered an FIF kit and an FDC kit, proceed as follows:

  a. Assemble the IFM as per the IFM ASSEMBLY INSTRUCTIONS (p. 2 - 17).

  b. Assemble the FIB as per the FIB ASSEMBLY INSTRUCTIONS (p. 3 - 23).

  c. Assemble the FPS as per the FPS ASSEMBLY INSTRUCTIONS (p. 5 - 29).

  d. Assemble the FLB as per the FLB ASSEMBLY INSTRUCTIONS (p. 6 - 17).

  e. Assemble the Floppy Cabinet as per the FLOPPY CABINET ASSEMBLY INSTRUCTIONS (p. 7 - 11).

  f. Turn to SYSTEM CONFIGURATION AND TESTING (p. 1 - 19).

IMSAI FLOPPY DISK SYSTEM

PART 1

SYSTEM MANUAL

FUNCTIONAL DESCRIPTION

The IMSAI Floppy Disk System provides for control of up to 4 flexible disk drives from the IMSAI 8080 System.

Data formats are fully compatible with the IBM 3740 format, providing a total storage capacity of 1.94 M bits per flexible disk. This is organized as 77 tracks with 26 sectors per track. Each sector contains 128 bytes of data.

To allow for non 3740 compatible formats, provision is made for reading all clock and data bits in an unformatted mode. The firmware may also be changed by reprogramming to support varying densities and formats.

The IMSAI Floppy Disk System utilizes an intelligent dedicated controller with a DMA capability to free the main processor from the overhead associated with floppy disk control processing.

Commands to the Floppy Disk System are initiated from the main processor by means of an output instruction to the controller (Byte Command). The actual command is executed from a command string located in the main system memory. Up to 16 different command string pointers may co-exist at any one time, with the values of these command string pointers being User definable.

SYSTEM COMPONENTS

The IMSAI Floppy Disk System consists of a Controller Set and a Drive Assembly.

The Controller Set is composed of two boards, the IFM (Interface Master) and the FIB (Floppy Interface Board).

The IFM is a separate 8080 based processor used to control floppy disk functions. It contains the 8080, 512 bytes of RAM, 2K bytes of EPROM, and all support logic for the 8080 chip. Communications with the main system processor takes place through the DMA channel or the single output port.

The FIB contains all the control logic necessary to drive the floppy disk from the IFM processor.

The Drive Assembly is composed of the Floppy Disk Drive, the Floppy Disk Cabinet, the FPS (Floppy Power Supply), the FLB (Floppy Light Board), and the PLO (data separator).

Each Floppy Cabinet houses up to two complete floppy drives with power supplies and a single FLB. In addition, the cabinet which houses Drive 0 contains a single PLO board which may be shared by up to 4 drives.

The Floppy Drive used in the system is the CalComp Model 140 providing up to 3.21 M bits of storage space (1.94 M bits with the IBM 3740 Format). Access times are 6ms track to track with a 10ms head stabilization.

The FPS provides all power needed to run the floppy disk drives and FLB. Provision is also made to terminate all control and signal lines from the Floppy Controller Set.

The PLO Board ensures a high level of data integrity and allows for the detection of missing clock patterns as used with the IBM 3740 Data and Address Marks.

SYSTEM THEORY OF OPERATION

THEORY OF OPERATION

PREFACE

This section is intended to help the User gain a general understanding of how the IMSAI Floppy Disk System functions as a whole. The operation of a theoretical floppy disk system is first presented to convey a general understanding of the principles involved in floppy disk transfers. Once this is achieved the operation of the IMSAI Floppy Disk System is explained.

Systems Operation does not cover the detailed logic and timing functions. If this information is desired the User should reference the Theory of Operations section for the individual system component.

I. FLOPPY DISK SYSTEMS IN GENERAL

A floppy disk system allows for the storage and retrieval of blocks of data between the main system memory and a storage medium, the floppy diskette.

The floppy disk system shown in Figure 1 provides the framework for a discussion of the processes involved in general floppy disk transfers. This floppy disk system is assumed to interface to a main processing system and is composed of two major elements:

1) a controller
2) a drive

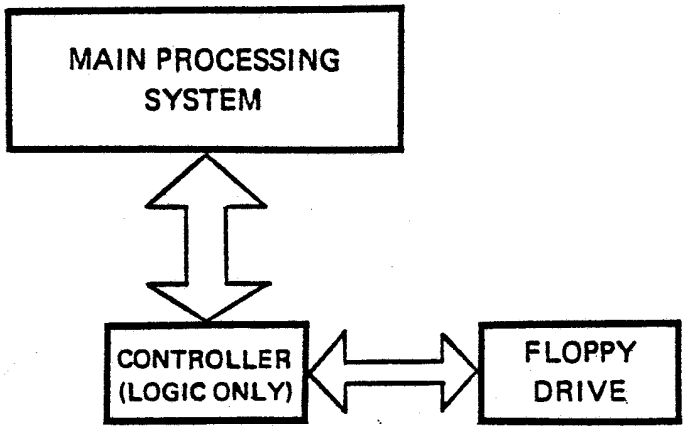


FIGURE 1, a simple floppy disk system

The controller contains all of the logic necessary to interface the floppy disk drive with the main processing system. All transfer routines are taken care of by the main processor. Note that control resides with the main processor only.

The drive contains the floppy disk storage unit which utilizes a moveable read/write head to access information stored on a flexible diskette.

DATA FORMATS

The data on the diskette is organized into tracks and sectors.

A track can be conceived of as a circular ring with its center located at the physical center of the diskette. If the read/write head is located a "distance" n from the center of the diskette, the nth track is defined as the area passing directly under the head in one complete revolution of the diskette.

Each track consists of a number of sectors. A sector is composed of preamble information, a data block, and postamble information. (See figure 2.)

A preamble information will normally contain: 1) a set pattern to indicate the start of a sector; 2) the track address; and 3) the sector address.

The data block contains the actual data transferred from the system's main memory.

The postamble information will normally include: 1) a number of check characters and 2) a gap to fill the end of a sector.

WRITE PROCESSES in a simple floppy disk system.

Assume there exists a block of data located in the system RAM which is to be stored on a floppy diskette. For simplicity, assume that the block size is equal to the sector data block size. In order to set up the transfer, the processor needs to get the address of the data block in system RAM and the location of the destination on the diskette (track and sector). Prior to executing the transfer, the processor needs to compute check characters for the block of data to be

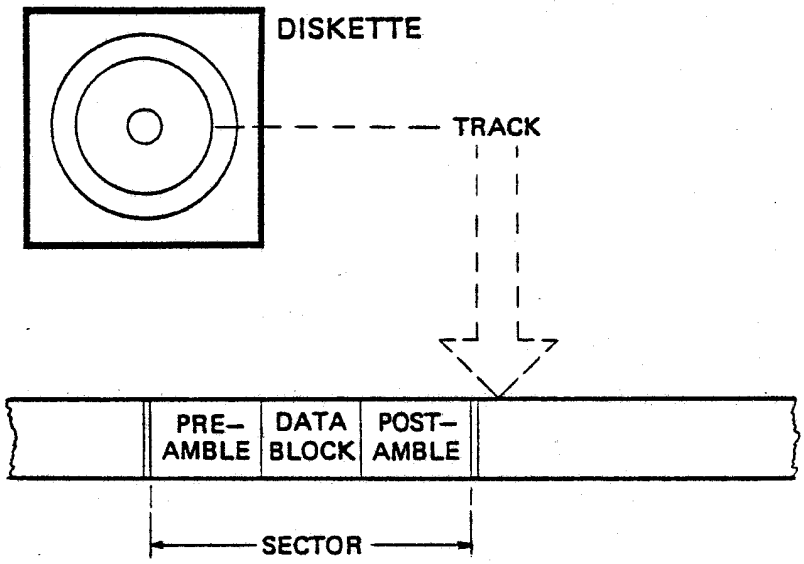


FIGURE 2, tracks and sectors

transferred. The check characters are used to verify the validity of the data when the block is read back into memory.

At this point the processor tells the floppy controller to position the head over the destination track and sector on the diskette. Once the floppy acknowledges it has positioned the head over the correct location, the processor sets the write enable and executes the transfer a word at a time until the block transfer is complete.

The check characters are then stored in the postamble, and the write enable is turned off. The process of writing onto the diskette is complete.

READ PROCESSES in a simple floppy disk system.

Transferring a block of data stored on diskette to the main processor's memory involves a similar process. The processor first needs to get the location of the data block on the diskette (track and sector) and the address of the destination in the system RAM.

The processor then commands the floppy to position the head over the desired track and sector. When the floppy acknowledges it has found the requested track and sector, the processor begins reading the data from the diskette into a previously defined storage area until the block read is complete.

The check characters (CRC) are then read and checked to insure the validity of the data. If the CRC is correct, the processor transfers the data from the storage area to the desired destination in the system RAM, thus completing the block read process.

ADDITIONAL HARDWARE FEATURES

With a basic understanding of the processes involved in floppy disc transfers, we can upgrade and improve the floppy disc system shown in figure 1 by:
1) using a separate processor in the controller; and
2) providing the controller with a DMA channel to the main system RAM.

Use of a separate processor in the controller to control floppy disc transfers will free up the main processor from the overhead associated with the previously discussed control processes and floppy housekeeping routines.

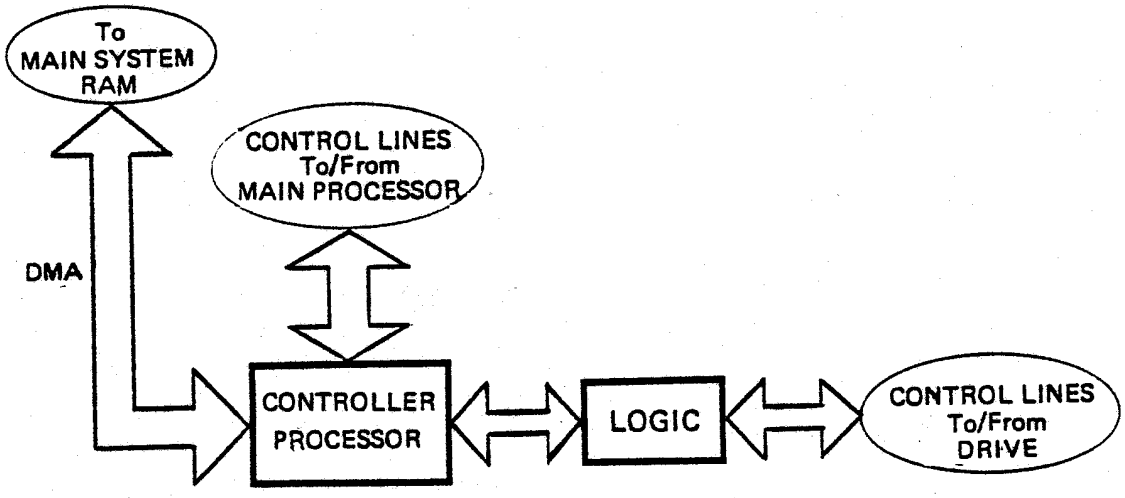


FIGURE 3, proposed floppy controller

Introducing a DMA channel into the proposed design of the controller allows for a direct access into the main system memory. The process of accessing system RAM then becomes essentially transparent to the main processor.

II. THE IMSAI FLOPPY DISK SYSTEM

The IMSAI Floppy Disk System consists of a Controller and Drive Assembly shown in figure 4.

The Controller contains an 8080 based processor and all logic necessary to interface up to four floppy disk drives from the 8080 microprocessor. The firmware, located in the Controller's 2K bytes of EPROM, contains the driving program for the IFM processor and supports the IBM 3740 Data Format.

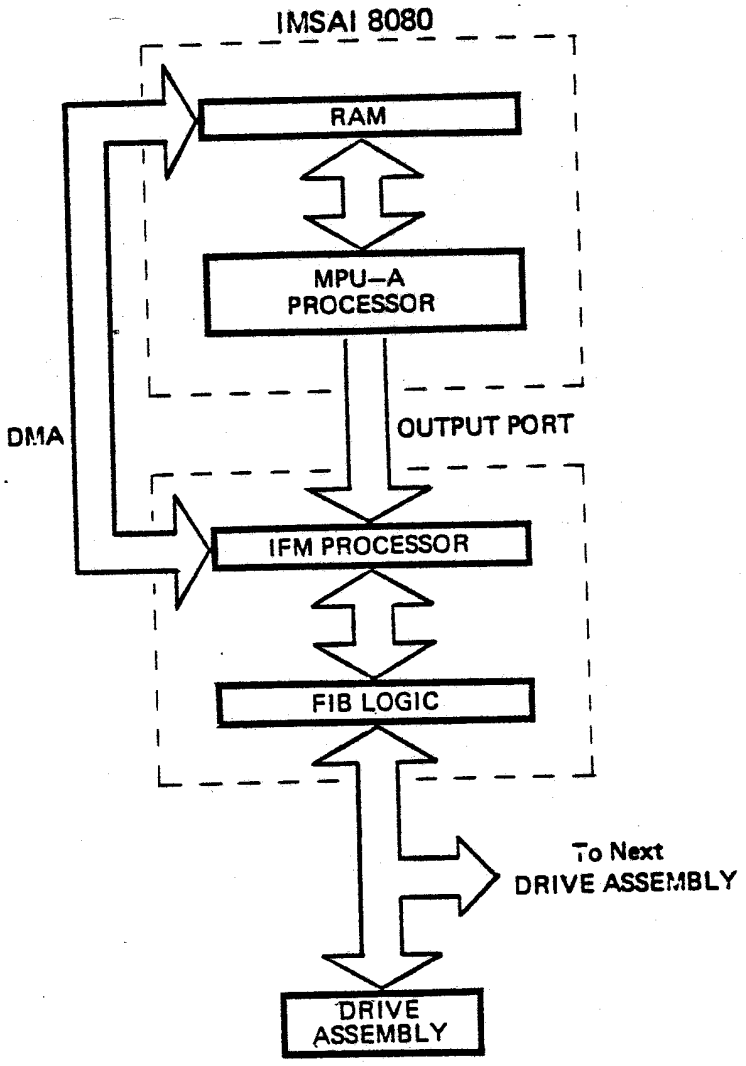


FIGURE 4, IMSAI Floppy Disk System

IBM 3740 FORMAT

The IBM 3740 format is organized into 77 tracks. Track 0 is used for Data Set Labels which contain descriptive information regarding data residing on tracks 01 through 76. Tracks 01 through 73 and 75 to 76 contain 26 sectors each with 128 data bytes per sector. Track 74 is not used.

Each data track has an Index Mark, a preamble, 26 sectors and a postamble. The organization of each sector is shown in figure 5. Both the ID Address Mark and the Data Address Mark consist of a particular pattern of missing clock pulses. These are used by the controller for synchronization.

For more detailed imformation refer to IBM publication GA21-9190.

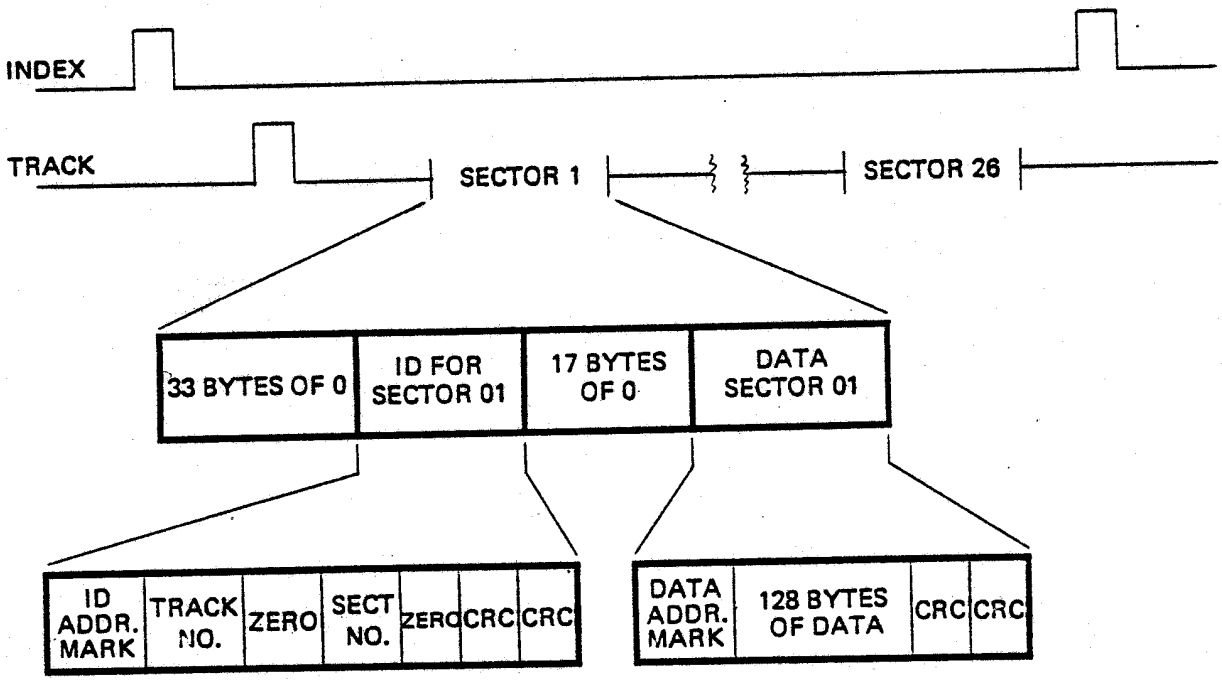


FIGURE 5, IBM Data Format

RECORDING FORMAT

In the IMSAI Floppy Disk System, both clocks and data are recorded on the disk utilizing a double frequency (FM) recording format. This format utilizes clocks to define bit cell times. The presence of a flux reversal between clocks is defined as a "one" bit. The absence of a flux reversal between clocks is defined as a "zero" bit. Figure 6 is an example of FM encoded data written on the disk.

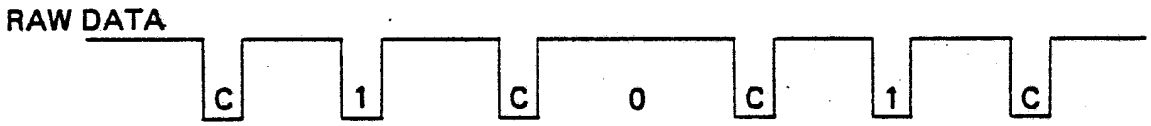


FIGURE 6, Raw Data

Data Recovery with the IBM 3740 Format

To allow recovery of data when using IBM 3740 formats, a PLO data separator is used. When synchronized, the PLO takes raw data from the disk and provides separated, coincident data and clock pulses to the FIB board. Figure 7 is an example of data and clock outputs from the PLO. A "one" bit may be detected as coincident pulses occurring on the data and clock lines.

Separated data and clock lines allow for the detection of ID and Data Address Marks which utilize a missing clock pattern. All missing clock patterns of significance in the 3740 format have a missing clock pulse in bit 5. Therefore, an ID or Data Address Mark is detected by checking for a missing clock pulse in this bit position.

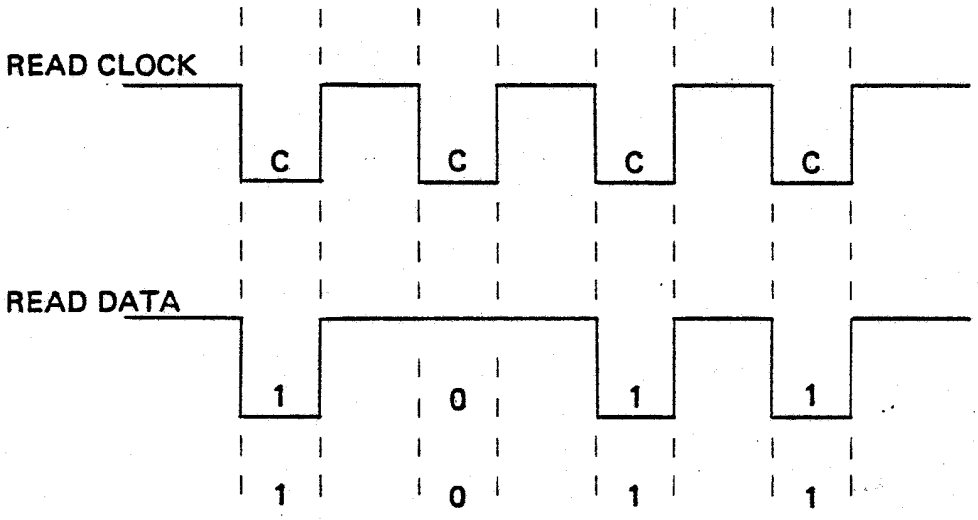


FIGURE 7, PLO outputs

MAIN PROCESSOR CONTROL OF FLOPPY DISK FUNCTIONS

Execution of a disk transfer operation is determined by Command Strings which reside in the main processor's memory. The execution of these Command Strings are initiated from the Main Processor by means of an output instruction.

The byte output to the IFM processor will contain a BYTE COMMAND number of 0 in the high 4 order bits and a pointer number to a particular Command String in the low 4 order bits.

Upon receipt of this Byte Command, the IFM processor will DMA the Command String pointed to in main memory and execute the command defined therein.

WRITE PROCESSES IN THE IMSAI FLOPPY DISK SYSTEM

MAIN SYSTEM PROCESSES

Assume there exists a block of data located in the main system RAM to be transferred to floppy disk. The main processor needs to first set-up the COMMAND STRING in main memory with 1) the command number for a sector write; 2) zero in the Status Byte; 3) the destination track and sector number and 4) the address in memory of the data block to be transferred.

The main processor then outputs a BYTE INSTRUCTION 0 to the IFM output port to initiate the execution of the write. The acknowledgement of a completed operation will be indicated by a non-zero value being stored in the status word of the COMMAND STRING. Thus once the processor issues the BYTE COMMAND 0, it only need wait for the status word to go non-zero before proceeding with another disk operation.

CONTROLLER PROCESSES

When the IFM board receives the output instruction (BYTE COMMAND 0), it lowers the Main Processor's READY line. The Main Processor goes into a WAIT state and the IFM Processor reads the output word from the system data bus into its own accumulator. Once the BYTE COMMAND is read the IFM Processor raises the System READY line to allow the SYSTEM to continue. The output word 0 is decoded by the IFM firmware as being a command to execute from the COMMAND STRING located in the System RAM.

DMA FUNCTIONS

The IFM processor will present a HOLD REQUEST to the System, and the System will respond with HOLD ACKNOWLEDGED. At this point the System is in a HOLD STATE and the IFM processor will disable all of the Main Processor's address, data, and status lines (with the exception of PHLDA). The IFM processor then gates its own address, data and status lines onto the System Bus.

The COMMAND STRING is now transferred to the IFM RAM from the System RAM, and the HOLD REQUEST is released, allowing the System to continue with its own processing activity.

The Command Number is decoded as a Write operation. The IFM processor transfers the Data block to the IFM RAM. This transfer is accomplished by DMA'ing a Byte at a time in the HOLD MODE during state T3 (or the state following T3) of the main processor's machine cycle.

To proceed with the WRITE operation, the IFM processor computes and stores the CRC characters in its own RAM.

TRACK POSITIONING

A request is issued to the FIB to load the head, sync the PLO, and then to synchronize on the ID Address Mark. The FIB then places the IFM Processor in a WAIT State until it has found the desired missing clock pattern.

Once the FIB has recognized the Address Mark, it raises the IFM READY line, allowing the IFM processor to read and check the track address. A compare is made to see if the head is positioned over the desired track. If not, the direction and Step lines are used to reposition the head over the destination track.

SECTOR POSITIONING

Once again the IFM Processor issues a request to the FIB to synchronize on the ID Address Mark. The IFM is again placed in a WAIT State until the ID Address Mark is recognized. Once the IFM is allowed to continue, it reads and checks track and sector number, this time looking for the destination sector. If the head is verified to be positioned over the desired sector, the IFM processor waits 12 bytes before writing the remaining five 0 bytes, the Data Address Mark, 128 bytes of data, and the 2 CRC characters according to the IBM 3740 Data Format.

COMPLETION OF THE OPERATION

At this point, the Write operation is complete and the IFM board will indicate the results of the operation to the Main System by storing a non-zero value in the Status Word of the COMMAND STRING, via the DMA channel.

READ PROCESSES IN THE IMSAI FLOPPY DISK SYSTEM

MAIN SYSTEM PROCESSES

To prepare for a Read operation the main processor sets up the COMMAND WORD in its RAM with:

1) The Command Number for a sector Read;
2) zero in the Status Byte;
3) the track and sector number for the data block to be read from the diskette;
4) the Address of the destination in Main memory.

The main processor then issues an output instruction (BYTE COMMAND 0) to initiate the READ operation. The main processor waits until the Status Byte of the COMMAND STRING goes non-zero before proceeding with another disk operation.

CONTROLLER PROCESSES

As before, the IFM processor will receive the output instruction from the main processor and decode it as an execute from COMMAND STRING.

The COMMAND STRING will be transferred from the System RAM to the IFM memory via the DMA access channel. The Command Number is decoded as a READ operation and the IFM processor positions the read/write head over the desired track and sector as before. Once the head is correctly positioned, the IFM processor waits for the Data Address Mark.

When the Data Address Mark is recognized, 128 bytes of data are read into the IFM RAM. The two CRC characters are then read and checked to verify the data block. If the data block is verified, it is written into the main processor's RAM via the DMA channel.

To acknowledge completion of the READ operation, the IFM processor will store a non-zero value in the Status Byte. This value is then passed to the COMMAND STRING located in the main system RAM via the DMA channel.

SYSTEM CONFIGURATION

AND TESTING

14860 Wicks Boulevard
San Leandro, California 94577

SINGLE DISK SYSTEM

FIF-1 CONSISTING OF:

1 IFM
1 FIB
1 CABLE A
1 CABLE C
1 CABLE F

1 CABINET
1 FPS (#0)
1 FLB (#0-1)
1 C140 DRIVE UNIT
1 CABLE E

ORDER:

1 FIF
1 FDC 2-1 (#0)

TWO DISK SYSTEM

FIF-1 AS PER ABOVE

1 CABINET
2 FPS (#0)
(#1)
1 FLB (#0-1)
2 CABLE E
2 C140 DRIVE UNITS

ORDER:

1 FIF 1 FIF
1 FDC 2-1 OR 1 FDC 2-2
1 FDC
(DRIVE 0,1)

THREE DISK SYSTEM

FIF-1 AS PER ABOVE

CABINET WITH 2 DRIVES AS PER ABOVE AND...

1 CABINET
1 FPS (#2)
1 FLB (#2-3)
1 C140 DRIVE UNIT
1 CABLE E
1 CABLE C

ORDER:

1 FIF 1 FIF
2 FDC 2-1 1 FDC 2-2
1 FDC OR 1 FDC 2-1
1 CABLE C

(DRIVE 0,1,2)

FOUR DISK SYSTEM

FIF-1 AS PER ABOVE

CABINET WITH 2 DRIVES AS PER ABOVE AND...

1 CABINET
2 FPS (#2)
(#3)
1 FLB (#2-3)
2 C140 DRIVE UNITS
2 CABLE E
1 CABLE C

ORDER:

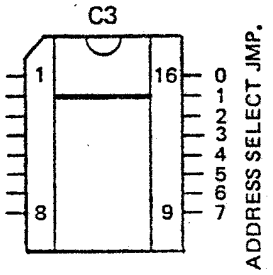
1 FIF 1 FIF
2 FDC 2-1 OR 2 FDC 2-2
2 FDC
1 CABLE C

(DRIVE 0,1,2,3)

IMSAI FLOPPY DISK SYSTEM CONFIGURATION GUIDE----------

The information here is presented to serve as a reference in configuring an IMSAI Floppy Disk System once its components have been assembled.

1. SET THE ADDRESS for the IFM output port by configuring the header for the address jumper socket in position C3 (IFM). IMSAI standard Floppy address is FD (Hex).



2. INSERT THE IFM AND FIB BOARDS into two slots in the IMSAI 8080 Motherboard.

3. IDENTIFY THE THREE CABLES used in the System as follows:

   CABLE A- CABLE A is a 12", 25 conductor cable with an EIA D Type connector on one end and a 26 pin board edge connector on the other end.

   CABLE C- CABLE C is a 3', 25 conductor cable with an EIA D Type connector on each end.
   NOTE: 3 and 4 Drive systems require 2-Cable C's.

   CABLE F- CABLE F is a 4", 50 conductor cable with a 50 pin board edge connector on each end.

4. ATTACH CABLE F between the IFM and FIB Boards. When attaching Cable F, verify that pin 1 on each connector corresponds to pin 1 on the board edge connector.

5. MOUNT THE EIA D TYPE CONNECTOR of Cable A to the rear of the 8080 chassis with the hardware provided.

6. ATTACH THE REMAINING END OF CABLE A to the FIB Board. The 26 pin edge connector mates with the edge connector located in the upper left hand corner of the FIB Board. Verify that pin 1 of the connector mates with pin 1 of the board edge connector.

IMSAI FLOPPY DISK SYSTEM CONFIGURATION GUIDE----------

SINGLE DRIVE SYSTEM

7. CONNECT CABLE C between the rear of the IMSAI 8080 chassis and the Floppy Drive Chassis as follows. Attach one end of Cable C to the D Type connector of Cable A. The remaining end will connect to the D Type connector located at the rear of the Floppy Chassis BEHIND DRIVE 0, (located on the right as you face the front of the Floppy Chassis).

TWO DRIVE SYSTEM

7. CONNECT CABLE C between the rear of the IMSAI 8080 chassis and the Floppy Drive Chassis as follows. Attach one end of Cable C to the D Type connector of Cable A. The remaining end will connect to the D Type connector located at the rear of the Floppy Chassis BEHIND DRIVE 0, (located on the right as you face the front of the Floppy Chassis).

THREE DRIVE SYSTEM

7. CONNECT ONE CABLE C between the rear of the IMSAI 8080 chassis and the Floppy Drive Chassis as follows: Attach one end of Cable C to the D Type connector of Cable A. The remaining end will connect to the D Type connector located at the rear of the Floppy Chassis, (containing Drives 0 and 1), BEHIND DRIVE 0, (located on the right as you face the front of the Floppy Chassis).

   CONNECT THE SECOND CABLE C between the two Floppy Drive Chassis' as follows. Attach one end of Cable C to the D Type connector BEHIND DRIVE 1, (located on the left as you face the front of the Floppy Drive Chassis containing Drives 0 and 1). The remaining end of this Cable C will connect to the D Type connector BEHIND DRIVE 2, (located on the right as you face the Floppy Drive Chassis containing Drive 2).

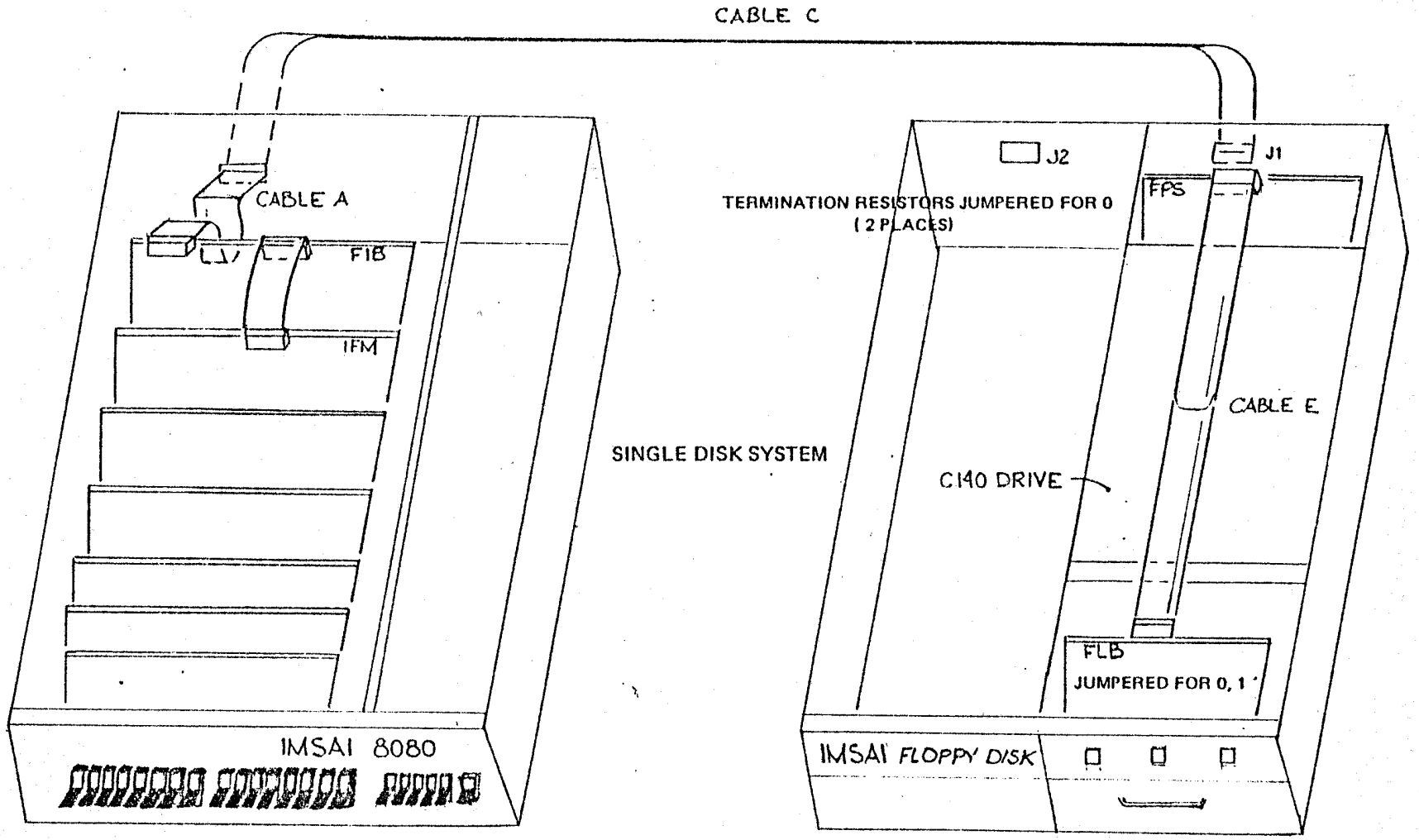
IMSAI FLOPPY DISK SYSTEM CONFIGURATION GUIDE----------

FOUR DRIVE SYSTEM

7. CONNECT ONE CABLE C between the rear of the IMSAI 8080 chassis and the second Floppy Drive Chassis as follows. Attach one end of this Cable C to the D Type connector of Cable A. The remaining end will connect to the D Type connector located at the rear of the Floppy Chassis, (containing Drives 0 and 1), BEHIND DRIVE 0, (located on the right as you face the front of the Floppy Drive Chassis).

   CONNECT THE SECOND CABLE C between the two Floppy Drive Chassis' as follows. Attach one end of this Cable C to the D Type connector located at the rear of the Floppy Chassis BEHIND DRIVE 2, (located on the right as you face the front of the Floppy Chassis containg Drives 2 and 3). The remaining end will connect to the D Type connector located at the rear of the Floppy Chassis BEHIND DRIVE 1, (located on the left as you face the front of the Floppy Chassis containing Drives 0 and 1).

THE IMSAI FLOPPY DISK SYSTEM IS NOW CONFIGURED AS REQUIRED FOR SYSTEM TESTING AND CP/M OPERATION.



THIS PORTION IS IDENTICAL FOR ALL DISK SYSTEMS.
FIF & CABLE C

8080 PARTS LIST

1 IFM
1 FIB
1 IFM–FIB CABLE
1 CABLE A
1 CABLE C
= FIF

UNIQUE TO SINGLE DISK SYSTEM

SINGLE DISK PARTS LIST

1 CABINET
1 FPS
1 FLB
1 C140 (DRIVE UNIT)
1 CABLE E
+ FIF

FLOPPY DISK SYSTEM
CONFIGURATION INFORMATION

SYSTEM INITIALIZATION----------

The following procedure should be used when powering up the System.

1. Insure that the diskettes are removed from the Drives.

2. Power up the 8080.

3. Connect the power cord from the Drive Assembly.

4. Insert a diskette in the Drive.

5. The following events should be observed:

   a. When the drive becomes Ready, a faint, audible click should be heard as the drive is restored by the Firmware.

   b. Status Lights: TRACK 00 should be active;
      WRITE ENABLED should be active;
      HEAD LOADED should be inactive;
      WRITE should be inactive.

   c. Ready and Select:
      Both SELECT's should be active.
      The READY should be active for the drive being used.

IF THESE EVENTS ARE NOT OBSERVED, check the following points:

   a. Check all supply voltages on the IFM and FIB Boards.
   b. Check and verify all cable connections.
   c. Check and verify the EPROM located in position A10 of the IFM Board (PROM00).
   d. Insure that an address jumper has been placed in socket C3 of the IFM Board.
   e. Check and verify that the IFM processor is in the RUN state (A1-3).
   f. If the problem still exists, use the firmware listing as a guide in troubleshooting the Scan Loop. The Scan Loop code begins at SCLP and is described in the FIB Firmware section under the heading STRAIGHT LINE DESCRIPTION OF THE PROGRAM.

SYSTEM TESTING----------

TEST MODULES

System testing described in this section consists of : 1) testing a single track format operation; 2) testing a sector write; 3) testing a sector read; and 4) testing the head positioning operation.

The test procedure is written so that the User must start with Test Module 1 to test single track format operations. Each succeeding module may be added to the existing code to test succeeding disk functions.

The complete test procedure requires 512 bytes of RAM beginning at address 1800H. The Command String resides at address 1880H, and the 128 byte buffer begins at 1800H.

If an error occurs when running the Test Modules, the Status Word in the Command String should indicate the type of error encountered. This information may be used to narrow down the possible sources of trouble given in the following section.

If the Status Word remains 0 when a failure occurs, the firmware has not completed, or perhaps even started, the operation. Check the DMA control circuits. Reference the IFM Theory of Operations.

TEST MODULE 1

1. Set the address jumper at C3 on the IFM board for the address FD (Hex).

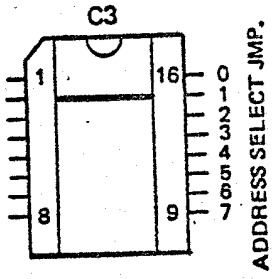


FIGURE 13, C3 Address Jumper (IFM)

2. Load the Test Module 1 beginning at 1889H.

3. RESET

4. EXAMINE 1889H.

5. Set the Drive Select Number in the Programmed Input Switches as follows:

   01H to select Drive 0
   02H to select Drive 1
   04H to select Drive 2
   08H to select Drive 3

6. Load the Diskette and close the door on the Drive. Wait for the Drive to come READY.

7. RUN.

When operating correctly, Track 0 is continuously formatted.

TEST MODULE 2

1. Load the Test Module 2 beginning at 18CDH.

2. Note that Test Module 1 MUST be loaded prior to using Test Module 2.

3. EXAMINE 1889H.

4. Set the Drive Select Number in the Programmed Input Switches.

5. Load the Diskette and wait for the Drive to come READY.

6. RUN.

Test Module 2 will Write from the buffer area at 1800H onto Track 0, Sector 1.

TEST MODULE 3

1. Load Test Module 3 beginning at 18E2H.

2. Test Modules 1 and 2 MUST be loaded prior to using Test Module 3.

3. EXAMINE 1889H.

4. Set the Drive Select Number in the Programmed Input Switches.

5. Load the Diskette and wait for the Drive to come READY.

6. RUN.

Test Module 3 will Read from Track 0, Sector 1 into the Buffer Area at 1800H.

TEST MODULE 4

1. Load Test Module 4 beginning at 18F0H.

2. Test Modules 1, 3 and 3 MUST be loaded prior to using Test Module 4.

3. EXAMINE 1889H.

4. Set the Drive Select Number in the Programmed Input Switches.

5. Load the Diskette and wait for the Drive to come READY.

6. RUN.

Test Module 4 will format Track 76 to test the head positioning routines.

ERROR DEBUGGING

If an error occurs when running Test Module 1, the following points should be checked.

GROUP 1

1. Check FIF blue wire modifications (IFM Rev. 2 and 3, FIB Rev. 2 and 3).

2. Check and verify that the diskette is not damaged.

3. Check and verify the firmware in the IFM PROM.

4. Check the OUTPUT COMMAND CONTROL CIRCUIT on the IFM board. Use the IFM Theory of Operation as a reference in troubleshooting.

5. If the Status Word in the Command String remains

0 when the failure occurs, or if the test program is lost/destroyed when running the test module, check the DMA CONTROL CIRCUIT. Use the IFM Theory of Operations as a reference in troubleshooting.

6. Insure that the address jumpers have been correctly configured in position C3 of the IFM board.

7. Check the LOAD CONTROL CIRCUITS on the FIB Board. Reference the FIB Theory of Operations.

8. Check the INDEX MARK DETECTION CIRCUIT on the FIB board. Reference FIB Theory of Operations.

9. Check the IFM RAM CHIPS B9 and B12.

IF AN ERROR OCCURS with the addition of Test Module 2, check all items listed in GROUP 1 and the following.

GROUP 2

1. Check the SYNCH READ DATA CIRCUIT on the FIB Board. Reference the FIB Theory of Operations.

2. Check the PLO operation and the PLO SYNCH circuit on the FIB Board.

IF AN ERROR OCCURS with the addition of Test Module 3, check all items in GROUPS 1, 2, and the following.

GROUP 3

1. Check the READ DATA CIRCUIT on the FIB. Reference the FIB Theory of Operations.

2. Check the BYTE DONE CIRCUITS on the FIB. Reference the FIB Theory of Operations.

IF AN ERROR OCCURS with the addition of Test Module 4, check all items in GROUPS 1, 2, 3, and the following.

GROUP 4

1. Check the Direction and Step Lines on the FIB Board. Refer to the CALCOMP OEM Manual for specs.

USE OF THE FIRMWARE LISTING IS RECOMMENDED AS A GUIDE IN TROUBLESHOOTING INDIVIDUAL DISK OPERATIONS.

```
                        ;
                        ;
                        ;       TEST MODULE 1
                        ;
                        ;       SETS UP THE COMMAND
                        ;       STRING AND FORMATS
                        ;
                        ;       TRACK 0
                        ;       VERSION 1.0  10/78
                        ;
                        ;
1800                            ORG   1800H
1800 =          BUFA    EQU   $
1800                            DS    128           ;BUFFER AREA
00FD =          IFMIO   EQU   0FDH          ;IFM I/O PORT
1880 =          CMD     EQU   $
1880                            DS    9             ;COMMAND STRING
1889 C39018             JMP   START         ;START PROGRAM
188C 97         ISSUE   SUB   A             ;ZERO ACC
188D D3FD               OUT   IFMIO         ;EXEC COMMAND
188F 3A8118     STLP    LDA   CMD+1         ;GET STATUS
1892 B7                 ORA   A             ;SET FLAGS
1893 CA8F18             JZ    STLP          ;WAIT FOR STATUS
1896 F0                 RP
1897 D3FF               OUT   0FFH          ;OUT ERROR STATUS
1899 C3B018             JMP   BEGIN
189C 31FB1B     START   LXI   S,1BFBH        ;SETUP STACK
189F 97                 SUB   A             ;ZERO ACC
18A0 328218             STA   CMD+2         ;ZERO BYTE 3 OF CS
18A3 210318             LXI   H,BUFA        ;GET BUFFER ADDR
18A6 228618             SHLD  CMD+5         ;STORE IN CS
18A9 3E10               MVI   A,10H
18AB D3FD               OUT   IFMIO         ;BYTE CMD 1
18AD 218018             LXI   H,CMD         ;GET CMD STR ADDR
18B0 7D                 MOV   A,L
18B1 D3FD               OUT   IFMIO         ;OUT LO CS ADDR
18B3 7C                 MOV   A,H           ;
18B4 D3FD               OUT   IFMIO         ;OUT HI CS ADDR
18B6 DBFF               IN    0FFH          ;INPUT DR. NO.
18B8 F620               ORI   20H
18BA D3FD               OUT   IFMIO         ;OUTPUT RESTORE CMD
18BC DBFF       BEGIN   IN    0FFH          ;GET DR. NO.
18BE F630               ORI   30H           ;FORMAT CMD.
18C0 328018             STA   CMD           ;STORE CMD NO.
18C3 97                 SUB   A             ;ZERO ACC
18C4 328118             STA   CMD+1         ;ZERO STATUS
18C7 328318             STA   CMD+3         ;ZERO TRACK
18CA CD8C18             CALL  ISSUE         ;ISSUE CMD
18CD C3B018             JMP   BEGIN
```

```
                        ;
                        ;
                        ;       TEST MODULE 2
                        ;
                        ;       WRITES TRACK 2
                        ;       VERSION 1.0 10/76
                        ;
                        ;
                        ;
180D                            ORG   180DH
1880 =                  CMD     EQU   1880H
188C =                  ISSUE   EQU   188CH
18BC =                  BEGIN   EQU   18BCH
180D DBFF                       IN    0FFH        ;IN DR. NO.
180F F610                       ORI   10H         ;OR IN WRITE CMD
18D1 328018                     STA   CMD         ;STORE CMD NO.
18D4 97                         SUB   A           ;ZERO ACC
18D5 328118                     STA   CMD+1       ;ZERO STATUS
18D8 328318                     STA   CMD+3       ;ZERO TRACK
18DB 3C                         INR   A
18DC 328418                     STA   CMD+4       ;SECTOR 1
18DF CD8C18                     CALL  ISSUE       ;EXEC CMD
18E2 03BC18                     JMP   BEGIN
```

```
                        ;
                        ;
                        ;       TEST MODULE 3
                        ;
                        ;       READS TRACK 0
                        ;       VERSION 1.0 10/76
                        ;
                        ;
18E2                            ORG   18E2H
1880 =                  CMD     EQU   1880H
188C =                  ISSUE   EQU   188CH
18BC =                  BEGIN   EQU   18BCH
18E2 DBFF                       IN    0FFH        ;GET DR. NO.
18E4 F620                       ORI   20H         ;OR IN READ CMD
18E6 328018                     STA   CMD         ;STORE CMD NO.
18E9 97                         SUB   A           ;ZERO ACC
18EA 328118                     STA   CMD+1       ;ZERO STATUS
18ED CD8C18                     CALL  ISSUE       ;EXEC CMD
18F0 C3BC18                     JMP   BEGIN
```

```
                        ;
                        ;
                        ;       TEST MODULE 4
                        ;
                        ;       FORMATS TRACK 76
                        ;       VERSION 1.0 10/76
                        ;
                        ;
18F0                    ORG   18F0H
1880 =          CMD     EQU   1880H
188C =          ISSUE   EQU   188CH
18BC =          BEGIN   EQU   18BCH
18F0 97                 SUB   A             ;ZERO ACC
18F1 328118             STA   CMD+1         ;ZERO STATUS
18F4 3E4C               MVI   A,4CH         ;TRACK 76
18F6 328318             STA   CMD+3         ;STORE TRACK IN CS
18F9 DBFF               IN    0FFH          ;GET DRIVE NO.
18FB F630               ORI   30H           ;OR IN FORMAT NO.
18FD 328318             STA   CMD           ;STORE CMD NO.
1900 CD8C18             CALL  ISSUE         ;EXEC CMD STR
1903 C3BC18             JMP   BEGIN
```

AND NOW----------

Once your System has passed the System Testing previously described, you may proceed in one of several ways.

* If you wish to bring up IMSAI CP/M, refer to the IMSAI CP/M USER MANUAL for further instructions.

* If you wish to write your own disk access programs, refer to the Programming Guide in the System User Guide section of this manual. In writing your own disk access programs, it is adviseable to read the System Theory of Operation to gain a general understanding of the System operation.

* If you wish to understand the operation of the System, the following sections of this manual may prove helpful.

  System Theory of Operation
  IFM Theory of Operation
  FIB Theory of Operation
  FIB Firmware Theory of Operation
  Cal Comp OEM Reference Manual for the Model 140 Drive.

SYSTEM USER GUIDE

14860 Wicks Boulevard
San Leandro, California 94577

CAUTION

Take Diskettes out of the drives during system power up or down to prevent any possible changing of data.

9/9/76

USER GUIDE----------

USER CONTROLS

POWER SWITCH: The AC power switch is located at the rear of each FPS. Assembled Drives are shipped with this switch in the power-on position.

LOADING AND REMOVING DISKETTES: In the center of the face of each Drive is a simple, thumb operated pushbutton which is depressed to allow the spring-loaded front cover to open. The Flexible Disk may then be inserted or removed as appropriate. The cover may then be closed manually.

NOTE: Remove the Diskette from the drive before power is applied to or removed from the Controller Boards.

LIGHT DISPLAY: The Light Display monitors the READY and SELECT Lines for each Drive in the cabinet. The states of the four signal lines TRACK00, HEAD LD, WRITE, and WRITE ENABLED are monitored for the selected Drive.

SELECT: A SELECT line will become active when the Controller raises the Select Line for the appropriate Drive. Both Select Lines will appear to be continuously active since the Controller uses these lines in a polling process to determine if a Drive has become Ready.

READY: This will become active when a diskette is loaded and the cover is closed on a selected Drive.

TRACK 00: The TRACK 00 line will become active when the Read/Write head on the selected drive is positioned over Track 00.

HEAD LOAD: The HEAD LOAD line will become active when the Controller issues a request to the selected Drive to load the Read/Write head.

WRITE: The WRITE line will become active when the Controller issues a command to the selected drive to enable the Write line.

WRITE ENABLED: The WRITE ENABLED line will become active when the selected Drive acknowledges that the loaded diskette is not write protected. Circuitry in the Drive to support this feature is not standard.

SYSTEM INITIALIZATION

The following procedure should be used when powering up the System.

1. Insure that the diskettes are removed from the Drives.
2. Power up the 8080.
3. Connect the power cord from the Drive Assembly.
4. Insert a diskette in the Drive.
5. The following events should be observed:
   a. When the Drive becomes Ready, a faint, audible click should be heard as the drive is restored by the Firmware.
   b. Status Lights: TRACK 00 should be active; WRITE ENABLED should be active; HEAD LOADED should be inactive; WRITE should be inactive.
   c. Ready and Select: Both SELECT's should be active. The READY should be active for the drive being used.

SYSTEM BOOTSTRAP (IFM REV 3 FIRMWARE ONLY)

A "bootstrap" is a short program which reads another program from some storage medium into system RAM and executes it. This simple, yet general procedure gives the user freedom to load in any kind of operating system s/he desires. The IMSAI Floppy Disk System bootstrap reads sector 1 of track Ø from drive Ø into system RAM at Ø-7F and then jumps to location Ø.

The following procedure should be used when bootstrapping from an IMSAI CP/M System Diskette.

1. Insure that the diskettes are removed from the drives.
2. Power up the 8080.
3. Power up the floppy disk drive.
4. Insert a system diskette in drive Ø.
5. When the drive becomes READY, press RESET.
6. Set the ADDRESS switches for ØØØØ and press EXAMINE. A "C3" should appear in the DATA lights.
7. Press RUN.

At this point, the operating system should be loaded and run.

If a hardware error occurs, the error code (see FIB Software section) will be displayed in the PROGRAMMED OUTPUT lights. The bootstrap will be retried until it is successful, or until it is stopped. If unable to bootstrap, check the points described at the end of the SYSTEM INITIALIZATION section.

If REV 3 Firmware is not available, a Bootstrap Simulator is described in the IMSAI CP/M Documentation.

PROGRAMMING GUIDE

A. Introduction

An Assembly Language Program stored in the 8080 System Memory is necessary to access the Floppy Disk. To use the IMSAI Floppy Disk System, the User must understand how to write such a program.

In order to accomplish this, the User may think of the Floppy Disk as a SINGLE OUTPUT PORT from the 8080 Microprocessor System.

The program which will access the Floppy Disk System utilizes TWO TYPES OF INSTRUCTIONS:

1. BYTE INSTRUCTIONS and

2. A COMMAND STRING INSTRUCTION.

BYTE INSTRUCTIONS are OUTPUT INSTRUCTIONS to the output port of the Floppy Disk System.

A COMMAND STRING is a series of consecutive words located in the System Memory.

The processes which need to take place within this program are described as follows.

START.....SET UP THE COMMAND STRING IN RAM FOR A PARTICULAR DISK OPERATION

ISSUE THE BYTE COMMAND (OUTPUT INSTRUCTION) TO INITIATE THE EXECUTION OF A DISK OPERATION

CHECK THE STATUS WORD IN THE COMMAND STRING FOR AN INDICATION THAT THE DISK OPERATION IS COMPLETE

END.....

The sections of the USER GUIDE which follow give the detailed information necessary to WRITE THE FLOPPY DISK ACCESS PROGRAM.

B. Command Types

Control of the IMSAI Floppy Disk System from the 8080 Microcomputer System is of two types: 1) the BYTE COMMAND and
2) the COMMAND STRING.

BYTE COMMAND instructions are directly executable and are passed to the IFM board from the Main Processor via an OUTPUT instruction.

COMMAND STRING instructions are indirectly executable and are stored in variable length COMMAND STRINGS in the Main System RAM.

A COMMAND STRING instruction is executed when a BYTE COMMAND of 0 is output to the IFM board. At that time the IFM processor will get the COMMAND STRING from the Main Processor's memory via the DMA channel and execute the instruction contained therein.

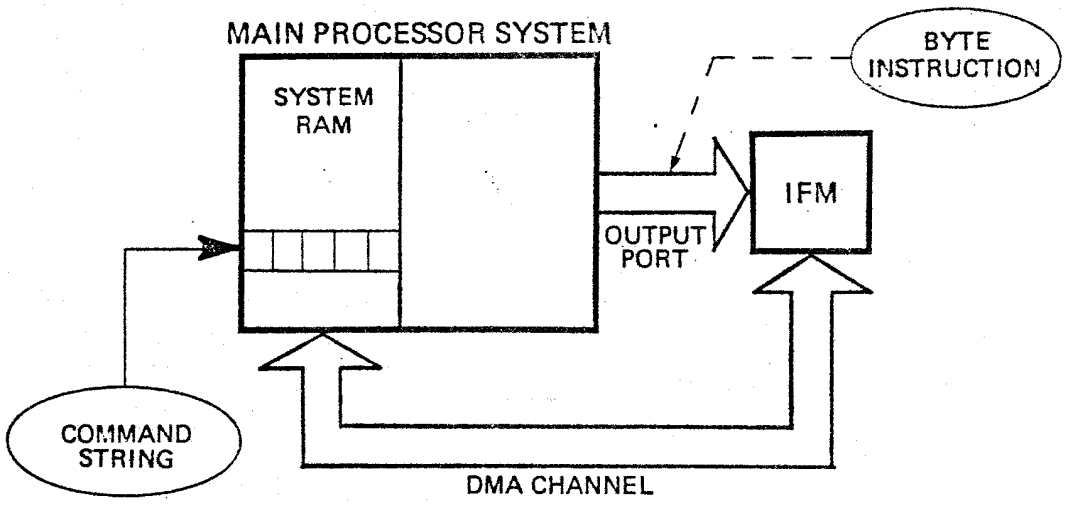


FIGURE 8, Control in the IMSAI FDS

C. BYTE COMMANDS

The Byte instruction is an eight bit word structured so that the upper four bits contain the BYTE INSTRUCTION NUMBER and the lower four bits contain either a pointer number or a drive select number, depending on the command used. (See figure 9.)

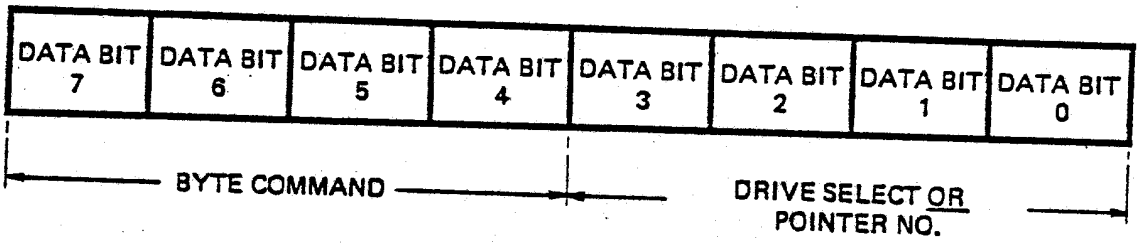


FIGURE 9, Byte Command

The Byte Instructions are listed below according to the Byte Instruction Number (the hex number contained in the upper four bits of the Byte Instruction).

COMMAND 0: Execute Command String from pointer. This command will take the pointer number from 0 to 15 and execute the Command String pointed to by that pointer. Note that prior to using this command the pointer address must have been initialized using Command 1.

COMMAND 1: This command will cause the floppy controller to take the next two bytes passed to it by the master microprocessor and use these as the new address for the pointer specified. Note that three bytes must be output to the IFM I/O port from the main processor to properly execute this command. (BYTE COMMAND NUMBER, LOW ORDER ADDRESS, HIGH ORDER ADDRESS)

COMMAND 2: Restore Drive causes the floppy controller to execute a restore command (position the head over track 0) on any or all drives selected.

COMMAND 3: Set Software Write Protect causes the controller to set a Write Protect on any of the drives which are selected. Note that in a power on condition, all drives come up WRITE ENABLED and therefore the WRITE PROTECT must be reset whenever power goes on.

COMMAND 4: Software WRITE ENABLE causes the microprocessor or the floppy controller to remove the WRITE PROTECT on any or all drives selected.

COMMAND 5 through COMMAND 15 perform no operation, except to reset interrupt if interrupt mode is being used. IMSAI standard RESET INTERRUPT command is command 5.

POINTERS

The pointer is a number from 0 to 15 which signifies that one of 16 addresses be used as the address of the Command String in Main Memory. Byte Commands 0 and 1 will take the lower four bits of the Byte Instruction Word as a pointer number to a Command String address. Note that Byte Command 1 is used to initialize the addresses of the pointers, while Byte Command 0 will execute the Command String pointed to by the lower four bits of the Byte Command Word.

On system power-up or RESET, the sixteen pointers are initialized with the following default values (all in hexadecimal).

Ø:	ØØ8Ø	4:	4ØØØ	8:	8ØØØ	C:	CØØØ
1:	1ØØØ	5:	5ØØØ	9:	9ØØØ	D:	DØØØ
2:	2ØØØ	6:	6ØØØ	A:	AØØØ	E:	EØØØ
3:	3ØØØ	7:	7ØØØ	B:	BØØØ	F:	FØØØ

DRIVE SELECT NUMBERS

Byte Commands 2, 3 and 4 will take the lower four bits of the Byte Instruction Word as a Drive Select number. A drive is selected (0-3) if its corresponding bit is a 1. A command with no drives selected does no operation.

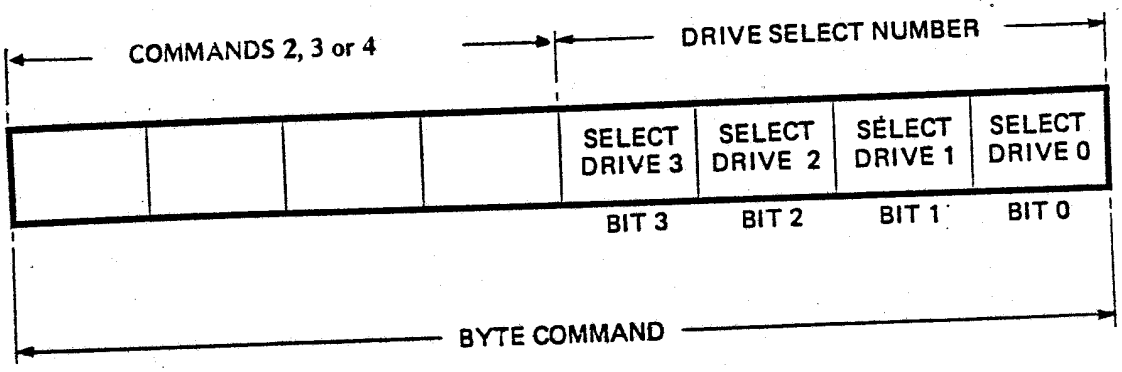


FIGURE 10, Drive Select Numbers

D. COMMAND STRING INSTRUCTIONS

Command String Instructions are indirectly executable and are stored in a variable length Command String in the Main System RAM.

The Command String is a series of from 4 to 9 consecutive 8 bit bytes in the main processor's memory. Its length or structure is dependant on the command used.

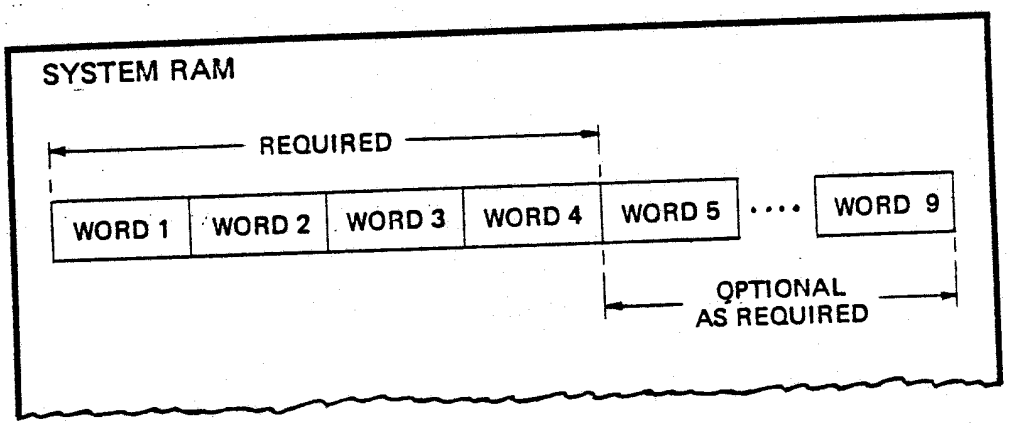


FIGURE 11, Command String Instructions

All Command Strings consist of at least four bytes of information. The definition of each 8 bit byte in the Command String is given below.

BYTE 1 - Command Byte

This byte contains a command number in the upper hexadecimal digit and the drive select number in the lower digit. The operation for each Command Number is defined in the next section and a drive is selected (0-3) if its corresponding bit is a one (bits 0-3).

BYTE 2 - Status Byte

This byte indicates to the master microprocessor the status of the present disk operation. It must be SET EQUAL TO 0 prior to executing the single Byte Command 0. This byte is set non-zero at the completion of the Command String by the IFM processor. If bit 7 is set, it indicates that the operation was not completed successfully. Bit 0 only is set on successful completion.

BYTE 3 and 4 - Track Address

Two Bytes are allowed for the track address for future expansion. At this time, Byte 3 must be 0, and Byte 4 contains a value from 0 - 76 to specify on what track the operation should be performed. Note that to maintain IBM media compatibility, it is possible to have the logical and physical track address differ. For commands to process this type of data, Bytes 3 - 4 contain the physical track address number.

Care must be exercised in operating with the logical and physical track address being different, and the user must be totally familiar with the format s/he is working with to perform any operation of this nature. For commands which specify no further track address, these two bytes contain both the physical and logical track address numbers.

BYTE 5 to 9

Bytes 5 to 9 of the Command String are defined according to the Command used.

COMMAND TYPES

The individual Command String commands are listed below by the command numbers - the upper four bits of the Command Byte.

COMMAND 0

The READ ALL command causes the IFM to delay the number of milliseconds contained in Byte position 5 from the physical index poles of the floppy disk and then to read 64 bytes. For each data byte, the corresponding clock byte is also read and is stored in the next sequential location in memory (i.e., stored are data from byte 1, clock from byte 1, data from byte 2, clock from byte 2, etc.). Hence, 128 bytes are transferred to the main processors memory at the data buffer location pointed to in Bytes 6 and 7. The delay in Byte 5 can be from 0 to 255 ms.

Note that the 64 bytes on the floppy disks consume approximately 2 ms and that software recognition for repositioning of the data is required to completely reconstruct the data pattern which is on the floppy disk. This command should be used with caution, and the user should be totally familiar with format contained on the floppy disk s/he is referencing before attempting to use the command. It is normally used only in cases of extreme difficulty or to decipher an unknown diskette format.

COMMAND 1

The WRITE SECTOR command causes the floppy controller to write the data from the location pointed to by Bytes 6 and 7. Byte 6 contains the least significant half of the data buffer location, and Byte 7 contains the most significant half. The data is written in the sector specified in Byte 5 (from 1 to 26).

COMMAND 2

READ SECTOR: The sector number contained in Byte 5 (from 1 to 26) is read and, upon successful completion of the read, the data is transferred to the data buffer location contained in Bytes 6 and 7. Byte 6 contains the least significant half of the data buffer location, and Byte 7 contains the the most significant half.

COMMAND 3

The FORMAT TRACK command uses no additional bytes and causes the floppy controller to write an IBM compatible format on the selected track number. This command destroys all previous information on the track and should be used with caution to initialize new diskettes.

COMMAND 4

The VERIFY SECTOR command causes the floppy controller to read and verify the redundancy check on the selected sector. NO DATA TRANSFER to the main processor's memory is initiated. Byte 5 for this command contains the sector number (from 1 to 26) which is to be verified.

COMMAND 5

The WRITE DELETED DATA SECTOR MARK command causes the floppy controller to write a deleted data mark in the data portion of the sector number contained in Byte 5. This command is used to indicate a defective sector, and the user should be completely familiar with the IBM format prior to initiating this command.

COMMAND 7 through 11

Commands 7 through 11 are identical with commands 1 through 5 and are used to read diskettes which have the logical and physical track address physically different. The logical track address to be used is always contained in the two bytes directly following the other command data called for in the COMMAND STRING (0-5). For example, if the basic command uses just 4 bytes, then the logical track number would be in bytes 5 and 6. If the basic command used 7 bytes, then the logical track address number would be in bytes 8 and 9.

The command will cause the controller to reference the physical track called out in bytes 3 and 4. But to compare the track address received off this physical track or to write the track address onto this physical track, it will use the logical track number contained in the appropriate bytes.

Note that up to 16 Command String Pointers may coexist in IFM memory at any one time. When a BYTE INSTRUCTION 0 is output to the IFM processor, the upper 4 bits of the BYTE INSTRUCTION will be the BYTE COMMAND NUMBER (in this case 0). The lower

4 bits will be the pointer number. The Command String to be taken from main memory and executed begins at the address contained in the specified pointer.

E. USE OF THE COMMAND STRING INSTRUCTIONS

Use of the Command String Instructions is detailed in the following discussion.

1. SET UP A POINTER TO A COMMAND STRING

By using Byte Command 1, the processor may set the value of a pointer. The processor will output a 1X to the IFM board where X is a pointer number (0-15). Following this will be an output of LL and then an HH where LL is the low order 8 bits and HH is the high order 8 bits of the address.

Once this is accomplished, the Command String beginning at address HHLL may be referred to by the pointer number X.

2. SET UP THE COMMAND STRING WITH ALL REQUIRED INFORMATION

a) Load the Command Number and Drive Select Number in BYTE 1.
b) Load a zero in the Status Byte (BYTE 2).
c) Load a zero in BYTE 3.
d) Load the track number in BYTE 4.
e) Load BYTES 5-9 as required by the operation being performed.

3. ISSUE A BYTE COMMAND 0 TO INITIATE THE EXECUTION OF A COMMAND STRING

The processor will output a 0X to the IFM board where X is a pointer number causing the Command String pointed to by X to be executed.

4. WAIT FOR THE COMPLETION FO THE OPERATION

The processor must wait for the Status Word to go non-zero before proceeding with another disk operation. If an error is indicated, the processor may at this time take appropriate actions.

EXAMPLES ARE GIVEN IN THE SECTION ON SYSTEM TESTING

F. ERROR SPECIFICATION FOR THE STATUS WORD

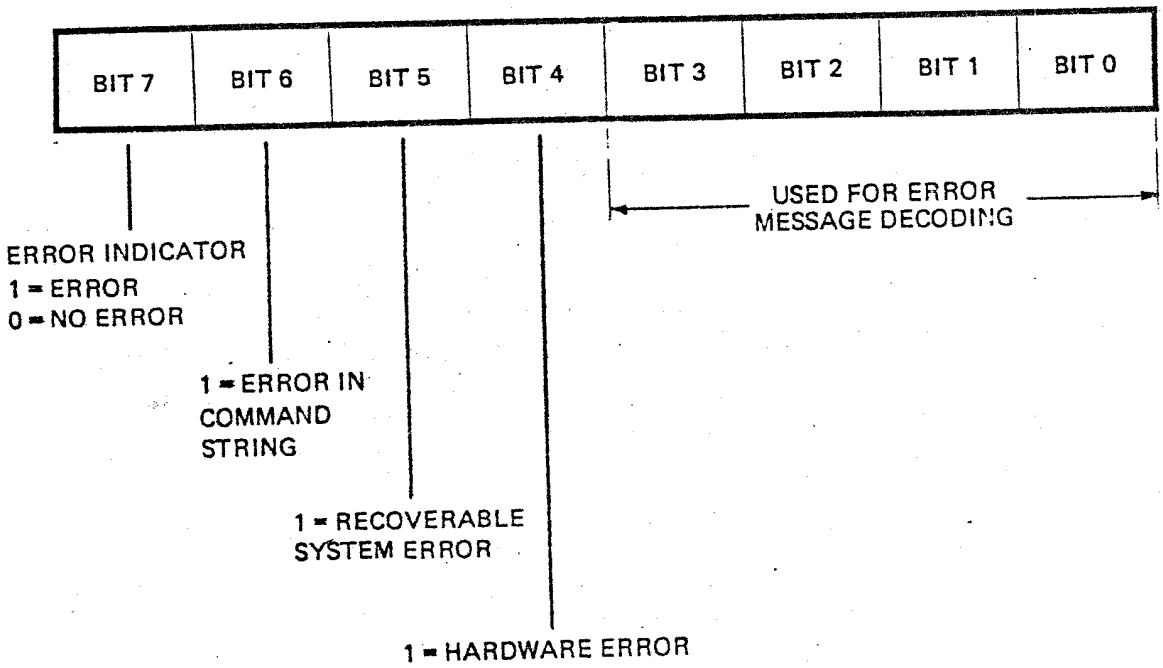


FIGURE 12, Status Word

If an error is indicated in the status word, BITS 6, 5, and 4 are used to identify the class of error as follows:

BIT 6

Bit 6, if set to a 1, indicates that an error was detected in the Command String. The individual error is specified by the least significant hexadecimal digit of the status response as follows:

IF SET TO a 1, it indicates that the Status Byte was not 0 upon initiation of the operation.

IF SET TO a 2, it indicates that no drive was selected.

IF SET TO a 3, it indicates that greater than one drive was selected.

IF SET TO a 4, it indicates an illegal command number was contained in the string.

IF SET TO a 5, it indicates that there was an illegal track address in the string.

IF SET TO a 6, it indicates that there was illegal sector address in the string.

IF SET TO a 7, it indicates that there was an illegal data buffer location in the string.

IF SET TO a 8, it indicates that there was illegal logical track address number in the string.

BIT 5

Bit 5, if set, indicates that there was a system error which may be recoverable by the operator. The low order digit is defined as follows:

IF SET TO a 1, it indicates that the selected drive was not ready for operation.

IF SET TO a 2, it indicates that the selected drive is hardware write protected, and an attempt to initiate a write operation on this drive was performed

IF SET TO a 3, it indicates that the selected drive is software write protected, and an attempt was made to initiate a write on this drive.

BIT 4

Bit 4, if set, indicates that there was a hardware malfunction which inhibited completion of the operation. The indicator digit is as follows:

IF SET TO a 1, it indicates that the selected drive is not operable; that is the controller was unable to position over track 0, or the drive went not ready during an operation.

IF SET TO a 2, it indicates that a track address error has occurred when attempting to read or write data onto the drive. An attempt is made 10 times to reposition the head over this track prior to indicating the error.

IF SET TO a 3, it indicates that a data synchronization error occurred; that is, the floppy controller was unable to find the selected sector number on the track prescribed within two revolutions.

IF SET TO a 4, it indicates that a CRC error occurred in the ID sector when attempting to locate the sector for read or write.

IF SET TO a 5, it indicates that there was a format error in the ID section when an attempt was made to locate the proper sector for a read or write.

IF SET TO a 6, it indicates that a CRC error occurred in the data portion of the sector when the data was read. Again this error is retried 10 times prior to submitting it to the processor as an error.

IF SET TO a 7, it indicates that a deleted data address mark was encountered when attempting to read data from the prescribed sector.

G. GENERAL NOTES ON ACCESSING THE DISK

Before writing on a new diskette the Format command must be used to write an IBM compatible format on the tracks to be used.

Note that tracks are numbered from 0 to 76 while sectors are numbered from 1 to 26. Also, note that these are decimal values.

To prevent possible damage to information stored on a diskette, remove the diskette from the drive BEFORE powering down the system.

IMSAI FLOPPY DISK SYSTEM

PART 2

COMPONENTS OF THE SYSTEM

FLOPPY DISK SYSTEM

CONTROLLER

IFM

FUNCTIONAL DESCRIPTION----------

The IMSAI Interface Master Board (IFM) is a complete 8080A based single board microcomputer configured as an intelligent interface controller. It is capable of interfacing, either directly or via minimal additional electronics, a wide variety of sophisticated peripheral equipment to an IMSAI 8080 Microcomputer System. The overhead normally associated with peripheral processing is eliminated from the system microprocessor (SMPU) since: 1. the IFM moves data between the SMPU and the peripheral via a DMA Channel; and 2. the IFM excercises routine control over the peripheral.

IFM I/O The SMPU communicates with the IFM via a bi-directional DMA Channel and an isolated output port. The electronics for both are implemented in the IFM and require no additional support circuitry. The DMA Channel normally gives the IFM access to the lower 32K bytes of the SMPU's memory. The isolated output port is normally used for issuing single byte commands to the IFM from the SMPU. Its address is jumper selectable and can range from 0 to 255_{10}.

DMA PRIORITY When used with other DMA devices, e.g. multiple IFM Boards, the DMA priority is resolved using a daisy chain scheme.

IMPLEMENTATION The IFM is implemented using an 8080A microprocessor, its support chips, 2K bytes of EPROM, 512 bytes of RAM, and the additional electronics required to interface to the SMPU busses. The IFM is powered by the IMSAI 8080 System and consumes one slot in the IMSAI 8080 backplane. External interface connections to peripherals or other interface boards are made via a 50 pin edge connector at the top of the Board.

THEORY OF OPERATION----------

The operation of the IFM Board is easily understood if it is broken down into its major functional blocks. The IFM consists of:

1. CPU Circuits,
2. On-Board Address Decoding,
3. Memory Circuits,
4. I/O Circuits,
5. DMA Circuits, and
6. DMA Priority Circuits.

CPU: The CPU employed by the IFM consists of an 8080A microprocessor, an 8224 System Clock, and an 8228 System Controller. This circuitry is described in detail in the Intel 8080 Microcomputer System User's Manual.

IFM ON-BOARD ADDRESS DECODING: IFM Address Lines MA10- MA15 are decoded by the 8205, located in position A5, to originate signals /E1 through /E8.

The 8205 is enabled when MA15, MA14, and MA13 are present on the IFM Address Bus in a low state. At this point, MA10 - MA12 are decoded to select one of the eight outputs /E1 - /E8, which are active low. Note that /INTA going low will disable the 8205.

The outputs /E1 - /E8 are used for gating and selecting on-board functions as listed in Table 1. They may also be used for external device and peripheral control functions, as /E4 - /E8 are available at the connector J2.

MEMORY: The IFM employs 2K Bytes of Eraseable Programmable Read Only Memory (EPROM) and 512 Bytes of Random Access Read Write Memory (RAM). The EPROM consists of two 8708 chips and the RAM consists of four 8111 chips.

On-board RAM is selected when the /E3 output of the 8205 (A5) goes low. This will occur when the address 08XX - 09XX appears on the IFM Address Bus.

The IFM RAM is organized as two blocks of 256x8 bit words. Each block of 256 is composed of two 4 bit half blocks since the organization of the 8111 is 256x4.

A RAM chip is selected when its inputs /CE1 and /CE2 are both low. Since the input of /CE2 is /E3 and the input to /CE1 is driven from MA8, an address of 08XX will select chips B9 and B12, while an address of 09XX will select chips B10 and B11.

Selection of an 8 bit word within a block of 256 is achieved through the use of MA0 - MA7. Output Disable and R/W inputs to the RAM chips are driven by /MEMR and /MEMW respectively.

The IFM PROM consists of two 8708 chips, organized as 1Kx8. PROM 0000, location A10, is enabled when /E1 goes active low. This will occur when an address in the range of 0000 - 03FF appears on the IFM Address Bus. Similarly, PROM 0400, location A11, is enabled when /E2 goes active low. This will occur when an address in the range of 0400 - 07FF appears on the IFM Address Bus. Selection of a word within each 1K block of PROM is achieved through the use of MA0 - MA9.

All of the IFM's memory (both EPROM and RAM) has less than 500 nanosecond access time so no WAIT states are used for memory references.

MA0-MA15 ADDRESS	SIGNAL	FUNCTION
0000-03FF	/E1	Enable PROM 0
0400-07FF	/E2	Enable PROM 1
0800-09FF	/E3	Enable RAM
0C00-0FFF	/E4	not assigned
1000-13FF	/E5	not assigned
1400	/E6	Command Data Port
1800	/E7	Command Status Port
1C00-1FFF	/E8	not assigned

TABLE 1. ON-BOARD ADDRESS DECODING

INPUT/OUTPUT: All I/O on the IFM Board is implemented using the Memory Mapped I/O technique. The I/O facilities consist of a single byte command port from the SMPU and any control ports implemented in the peripheral or external interface circuitry (e.g. FIB or LIB boards). The DMA channel can be viewed as 32K I/O ports but because of the extensive circuitry involved, it will be considered separately.

As viewed from the SMPU, the single byte command port is an isolated output port. When the SMPU outputs to this port, the address is decoded by the 7485 Comparators (C4 and C5) causing PADR to go high. This is gated with PWR and SOUT by a 74LS11 AND gate (B3), whose output CIN is high if and only if the SMPU is outputting to this port. CIN is connected to the STB input of the 8212 8-bit Latch (C8) and causes the data on the SMPU Data Bus to be loaded into the latch. This, in turn, sets the 8212 Internal Service Request Flip/Flop, causing /IORQ to go low and a Hold Request to be initiated. (Hold Request and DMA logic is discussed below).

As viewed from the IFM CPU, the single byte command port consists of a Memory Mapped Status Input Port and a Memory Mapped Data Input Port. The Status Port address is fixed at 1800H. When 1800H is decoded by the 8205 (A5), it causes /E7 to go low. This in turn, places IORQ on bit 0 of the Data Bus. (The remaining 7 bits of the status port are not used and their states are undefined.) IORQ being high indicates that a byte has been loaded into the 8212 (C8).

The Memory Mapped Data Input Port address is fixed at 1400H. When 1400H is decoded by the 8205 (A5), it causes the signal /E6 to go low. This enables the Tri-State outputs of the 8212, allowing the CPU to read the contents. /E6 also resets the 8212 Service Request Flip/Flop, causing /IORQ to go high and the associated Hold Request is removed.

Control I/O ports may be implemented in the peripheral equiptment or external interface circuitry. This is possible since all of the IFM's busses are available at the J2 connector.

DIRECT MEMORY ACCESS: As viewed from the IFM CPU, the DMA Channel can be considered to be 32K Memory Mapped I/O Ports. Alternately, it can be considered as a virtual extension of the IFM memory. A read or write in the upper 32K bytes of the IFM address space causes a DMA read or write in the lower 32K bytes of the SMPU address space. This can be changed to the upper 32K bytes of the SMPU address space under IFM program control, if the requisite latch is implemented on an additional board (e.g. LIB or FIB).

A DMA transaction is initiated when MA15 is high and either /MEMR or /MEMW is low. The IFM CPU is put into a Wait State, (RDYIN pulled low), and a Hold Request is initiated, (A2-11 goes high).

If /IORQ and /PRIIN are high, the CLR input to the shift register at A3 goes high. At this point, the 74195 shift register, A3, is in the LOAD mode. If /PHOLD is not currently being pulled low by another DMA device, the output Q_a of A3 is latched high on the trailing edge of the SMPU Ø2 clock, (SØ2). The output Q_a of A3 drives /PHOLD active low.

The SMPU acknowledges its entry into the HOLD State by driving PHLDA high. This, in turn, latches the Q_b output of A3 high. The SMPU Drivers are disabled at this time and the IFM drives the SMPU Address, Control, and Status Busses.
Note: When a byte is output to the single byte command port, a sequence of actions occurs similar to that which put the SMPU into a Hold.

Since the Q_b output of A3 is high, the signal, DMA, (A2-6) goes high, placing the 74195, A3, into the SHIFT Mode. The 8216 Bi-Directional Bus Drivers, (C6 and C9), are also enabled at this time, with the direction of the data transfer determined by /MEMR.

On the next trailing edge of SØ2, the Q_c output of A3 goes high, driving PWAIT high. /PWR is also driven low at this time if a write operation is to be executed.

One SØ2 period later, the Q_d output of A3 goes high. At this time PRDY is gated to drive RDYIN. Thus the IFM CPU resumes operation when PRDY is high. The DMA transaction terminates when both /MEMR and /MEMW are high.

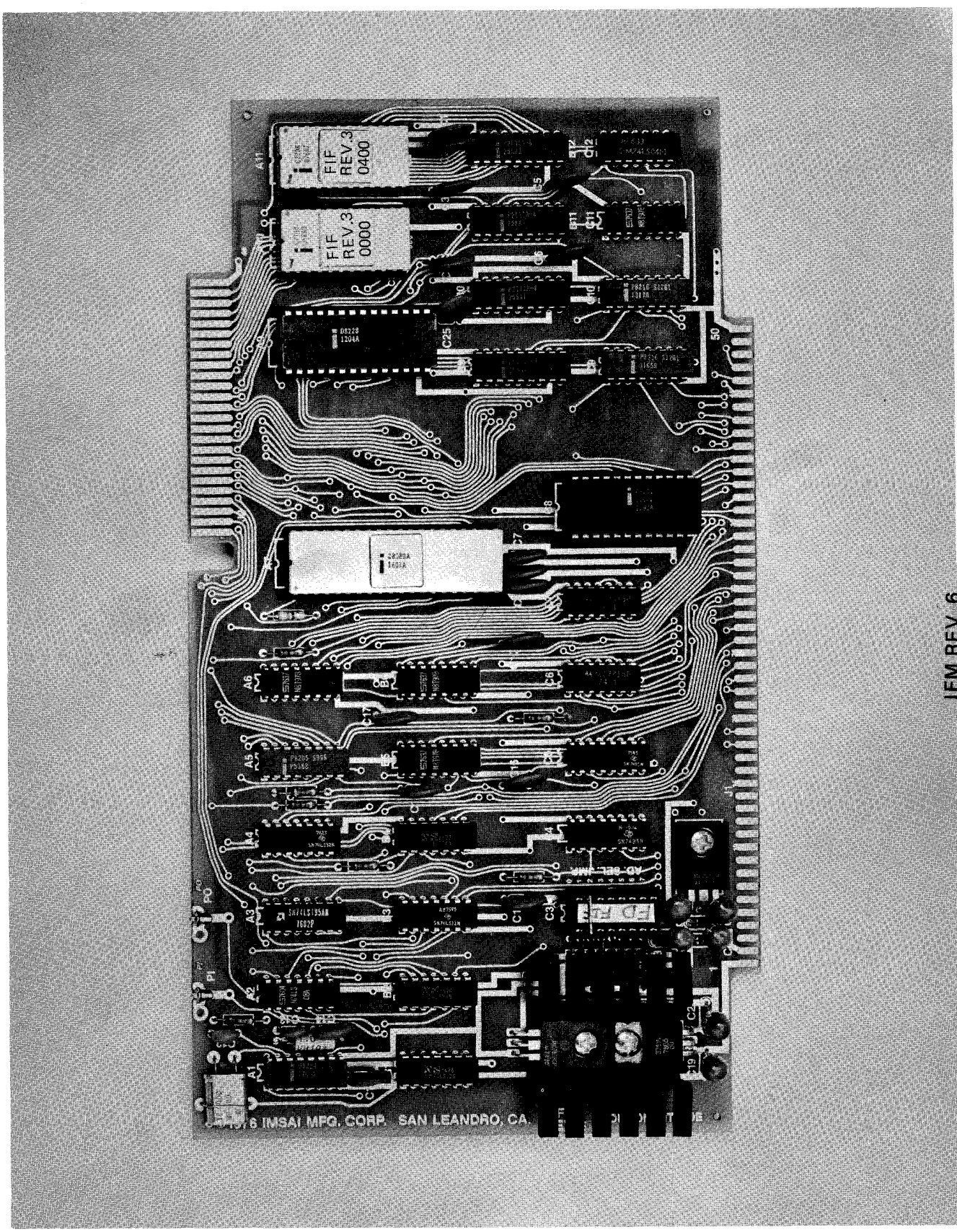
If, at the end of the DMA transaction, /IORQ is high, the CLR input to A3 goes low and control of the Busses is returned to the SMPU. /PHOLD goes high. The SMPU ceases Holding and resumes normal operation until the next DMA operation.

If, at the end of a DMA transaction, /IORQ is low, a single byte command is pending and the CLR input to A3 remains high. Since the DMA REQ, A2-11, is now low, DMA, A2-6, goes low and the 74195 shift register, A3, returns to the LOAD Mode. The first two bits of A3 remain high, but the second two bits go low. The SMPU continues to Hold. The 74195 remains in this state until /IORQ goes high or another DMA transaction is initiated. Thus, the SMPU is held after outputting a byte to the IFM until the IFM CPU reads the byte. The IFM is able to continue DMA operation during this time and will DMA slightly faster since it no longer is delayed by waiting for PHLDA.

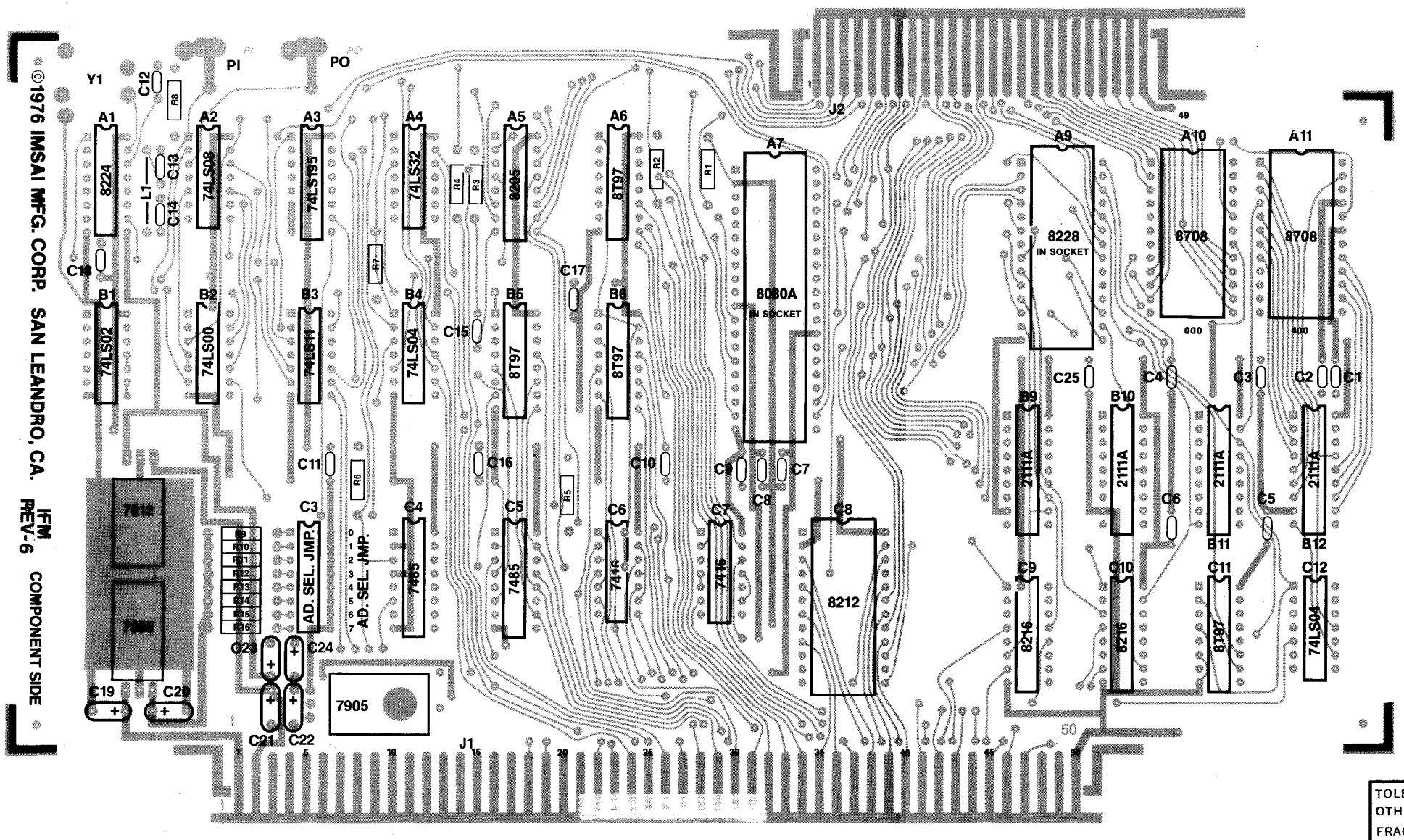
DMA PRIORITY: Conflicts for DMA access by multiple DMA channels is resolved using a daisy chain scheme. The /PRIOUT output of a DMA Controller is connected to the /PRIIN input of the controller with the next lowest priority. The /PRIIN input of the highest priority controller is left open and is pulled up by an on-board 1K resistor.

A controller pulls its /PRIOUT low if its /PRIIN input is low or if that controller is executing a DMA transaction. /PRIIN low indicates that a higher priority controller is executing a DMA transfer. Any pending DMA request must be delayed until /PRIIN returns high and /PHOLD is high.

If /PRIIN and /PHOLD are high, the IFM may initiate a DMA transaction by pulling /PHOLD low synchronized to the trailing edge of the SMPU Ø2 Clock. Simultaneously, /PRIOUT is pulled low. If /PRIIN remains high until the next trailing edge of SØ2, no higher priority DMA device requires service, and the DMA transaction may continue. However, if /PRIIN is pulled low, a higher priority channel requires service and the transaction must be aborted. DMA priority applies only to DMA transactions initiated on the same trailing edge of SØ2. All other DMA transactions are serviced on a first-come first-served basis. Once a DMA transaction is in progress, higher priority controllers must not initiate a DMA transaction or system malfunction will occur.


FIF
REV.3
0400
FIF
REV.3
0000
IFM REV. 6
FOR FIF

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL	11/76	djk



NOTES:

A10 & A11 with 24 pin sockets.
A9 with 28 pin socket.
A7 with 40 pin socket.
C3 with 16 pin socket.
Capacitors C19 through C24 are 33uF.
Capacitors C1 through C11, C14 through C18 & C25 are .1 uF.
Capacitor C12 is 39 pF.
Capacitor C13 is 56 pF.
Resistors are ¼ Watt.
Resistor R1 is 470.
Resistors R2 & R4 through R8 are 1K.
Resistor R3 is 4.7K.
Resistors R9 through R16 are 2.2K .
Inductor L1 is 1.0 uH.
Crystal Y1 is: 18 MHz for FIF,
16.129 MHz for LIF.
EPROM for A10 is 0000,
A11 is 0400.

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC.	ANGLES
±	±	±

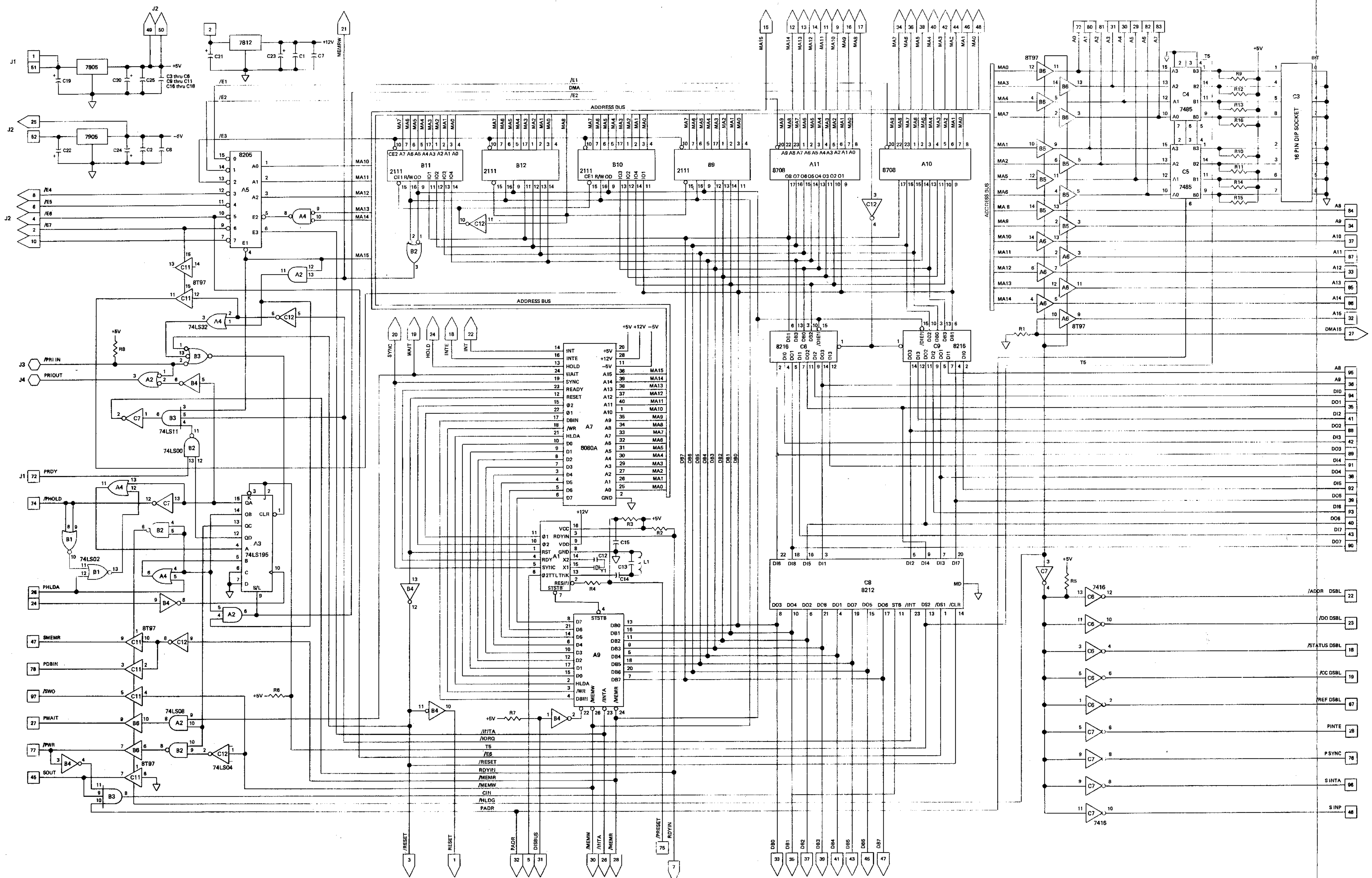
APPROVALS	DATE
DRAWN PEW	11/16/76
CHECKED	

ASSEMBLY DIAGRAM
IFM REV. 6 11/76

SCALE	SIZE	DRAWING NO.
	B	

DO NOT SCALE DRAWING | SHEET

LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL REV. 6	11/76	



A1	8224
A2	74LS08
A3	74LS195
A4	74LS32
A5	8205
A6	8T97
A7	8080A
A9	8228
A10, A11	8708
B1	74LS02
B2	74LS00
B3	74LS11
B4	74LS04
B5, B6	8T97
B9, B10, B11, B12	2111A
C1	7805
C3	ADD. SEL. JMPRS.
C4, C5	7485
C6, C7	7416
C8	8212
C9, C10	8216
C11	8T97
C12	74LS04
R1	470 ¼W
R2	1K ¼W
R3	4.7K ¼W
R4 thru R16	1K ¼W
R9 thru R16	2.2K ¼W
C1 thru C11	.1 uF
C12	39 pF
C13	56 pF
C14 thru C18, C25	.1 uF
C19 thru C24	33 uF
L1	1.0 uH
Y1	XTAL

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS ± DEC. ± ANGLES ±

APPROVALS | DATE
DRAWN
CHECKED

IMSAI MFG. CORP.
SAN LEANDRO, CA.

SCHEMATIC DIAGRAM
IFM-FIF REV. 6 11/76
IFM-LIF REV. 6 11/76

SCALE | SIZE | DRAWING NO
DO NOT SCALE DRAWING | SHEET

BOARD: IFM Rev. 6

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
Solder	15-0000001	10'	
Heat Sink	16-0100004	1	Thermalloy/6072-B
Screw	20-3202001	1	6-32x¼" Phillips Pan Head Machine
Screw	20-3302001	2	6-32x5/16" Phillips Pan Head Machine
Lockwasher	21-3350001	3	#6 Internal Star
Nut	21-3120001	3	6-32 Hex
Socket	23-0800001	1	16-Pin Solder Tail
Header	23-0400001	1	16-Pin IC Header
Socket	23-0800002	2	24-Pin Solder Tail
Socket	23-0800003	1	28-Pin Solder Tail
Socket	23-0800004	1	40-Pin Solder Tail
Socket Pin	23-0900007	2	Cambion #450-370401-04 (or -03 or -06)
Inductor	29-0400001	1	1uH/WEE 1.0
Resistor	30-3470362	1	470 Ohm, ¼ Watt/yellow, violet, brown
Resistor	30-4100362	6	1K Ohm, ¼ Watt/brown, black, red
Resistor	30-4220362	8	2.2K Ohm, ¼ Watt/red, red, red
Resistor	30-4470362	1	4.7K Ohm, ¼ Watt/yellow, violet, red
Capacitor	32-0239010	1	39pF Disk Ceramic
Capacitor	32-0256010	1	56pF Disk Ceramic
Capacitor	32-2010010	17	.1uF Disk Ceramic
Capacitor	32-2233070	6	33uF, 25V Tantalum
8T97	36-0089701	4	Hex Tri-State Buffer/N8T97B
74LS00	36-0740002	1	Quad 2-Input NAND(Low Power Schottky)/ SN74LS00N

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
74LS02	36-0740202	1	Quad 2-Input AND (LPS)/SN74LS02N
74LS04	36-0740402	2	Hex Inverter (LPS)/SN74LS04N
74LS08	36-0740802	1	Quad 2-Input AND (LPS)/SN74LS08N
74LS11	36-0741101	1	Triple 3 Input AND (LPS)/SN74LS11N
7416	36-0741601	2	Hex Inverter Driver, Open Collector/ 9N16/ 7416
74LS32	36-0743202	1	Quad 2-Input OR (LPS)/SN74LS32N
7485	36-0748501	2	4 Bit Magnitude Comparator/SN7485N
7805	36-0780501	1	Regulator/7805CU
7812	36-0781201	1	Regulator/FUA7812UC
7905	36-0790501	1	Regulator/MC7905CP
8080A	36-0808001	1	Microprocessor/C8080A
8111	36-0811101	4	256x4 Static MOS RAM/P8111 (or P2111)
8205	36-0820501	1	High Speed Binary Decoder /P8205
8212	36-0821201	1	8 Bit Input/Output Port/P8212
8216	36-0821601	2	4 Bit Bi-Directional Bus Driver/P8216
8224	36-0822401	1	Clock Generator and Driver/PB8224D
8228	36-0822801	1	System Controller and Bus Driver/D8228
74LS195	36-7419502	1	4 Bit Parallel In/Out Shift Register (LPS)/ DM74195N
Cable	91-0400007	1	Cable F Assembly
PC Board	92-0000021	1	IFM Rev. 6
FIF PROMs	88-0000006	1	Includes: 1 8708 Programmed FIF 0000 Rev. 3 1 8708 Programmed FIF 0400 Rev. 3
Crystal	35-5000003	1	18.00 MHz Crystal
Cable	91-0400003	1	Cable A Assembly

ASSEMBLY INSTRUCTIONS

( ) 1. Unpack your board and check all parts against the parts list enclosed in the package.

( ) 2. If gold contacts on the edge connectors appear to be tarnished, use a pencil eraser to remove any oxidation. NOTE: Do not use Scotchbright or any other abrasive material as it may remove the gold plating.

IC INSTALLATION

NOTE: All Pin 1's point toward the upper left hand edge of the board. Pads for Pin 1's are square.

( ) 3. Insert and solder the one 8224 at location A1 as shown on the Assembly Diagram.

( ) 4. Insert and solder the one 74LS08 at location A2 as shown on the Assembly Diagram.

( ) 5. Insert and solder the one 75LS195 at location A3 as shown on the Assembly Diagram.

( ) 6. Insert and solder the one 74LS32 at location A4 as shown on the Assembly Diagram.

( ) 7. Insert and solder the one 8205 at location A5 as shown on the Assembly Diagram.

( ) 8. Insert and solder the four 8T97's at locations A6, B5, B6 and C11 as shown on the Assembly Diagram.

( ) 9. Insert and solder the one 74LS02 at location B1 as shown on the Assembly Diagram.

( ) 10. Insert and solder the one 74LS00 at location B2 as shown on the Assembly Diagram.

( ) 11. Insert and solder the one 74LS11 at location B3 as shown on the Assembly Diagram.

( ) 12. Insert and solder the two 74LS04's at locations B4 and C12 as shown on the Assembly Diagram.

( ) 13. Insert and solder the four 8111's (or 2111's) at locations B9 through B12 as shown on the Assembly Diagram.

( ) 14. Insert and solder the two 7485's at locations C4 and C5 as shown on the Assembly Diagram.

( ) 15. Insert and solder the two 7416's at locations C6 and C7 as shown on the Assembly Diagram.

( ) 16. Insert and solder the 8212 at location C8 as shown on the Assembly Diagram.

( ) 17. Insert and solder the two 8216's at locations C9 and C10 as shown on the Assembly Diagram.

( ) 18. Insert and solder the one 40 pin socket at location A7 as shown on the Assembly Diagram.

( ) 19. Insert and solder the one 28 pin socket at location A9 as shown on the Assembly Diagram.

( ) 20. Insert and solder the two 24 pin sockets at locations A10 and A11 as shown on the Assembly Diagram.

( ) 21. Insert and solder the one 16 pin socket at location C3 as shown on the Assembly Diagram.

RESISTOR INSTALLATION

( ) 22. Insert and solder the one 470 Ohm, ¼ Watt resistor (yellow, violet, brown) at location R1 as shown on the Assembly Diagram.

( ) 23. Insert and solder the six 1K Ohm, ¼ Watt resistors (brown, black, red) at locations R2 and R4 through R8 as shown on the Assembly Diagram.

( ) 24. Insert and solder the one 4.7K Ohm, ¼ Watt resistor (yellow, violet, red) at location R3 as shown on the Assembly Diagram.

( ) 25. Insert and solder the eight 2.2K Ohm, ¼ Watt resistors (red, red, red) at locations R9 through R16 as shown on the Assembly Diagram.

DISCRETE COMPONENT INSTALLATION

( ) 26. Insert and solder the seventeen .1uF disk ceramic capacitors at locations C1 through C11, C14 through C18 and C25 as shown on the Assembly Diagram.

( ) 27. Insert and solder the one 39 pF disk ceramic capacitor at location C12 as shown on the Assembly Diagram.

( ) 28. Insert and solder the one 56pF disk ceramic capacitor at location C13 as shown on the Assembly Diagram.

( ) 29. Insert and solder the six 33uF tantalum capacitors at locations C19 through C24 as shown on the Assembly Diagram.
NOTE: Observe polarity (+ to +) as indicated on the board.

( ) 30. Insert and solder the one 1.0uH inductor coil at location L1 as shown on the Assembly Diagram.

( ) 31. At this time insert and solder the crystal (Y1). Use the two pads next to the legend C12. Make sure that the leads are long enough to allow the crystal to lay on its side flat against the board. Place a piece of electrical tape over the single pad which is completely under the crystal, then use a cut resistor lead soldered to the two pads at the edges of the crystal to hold the crystal down against the board. Refer to the photo.

REGULATOR AND HEAT SINK INSTALLATION

( ) 32. Bend the leads of the 7805, 7812 and 7905 regulators at 90 degree angles approximately ¼" from the bottom edge of the regulator to facilitate insertion. The bends should be away from the side bearing the regulator number.

( ) 33. Insert the 7812 regulator at the top of the heat sink. Attach securely with a 6-32x5/16" machine screw from the component side and a #6 lockwasher and nut on the solder side. Ensure that the heat sink is positioned with its sides parallel to the sides of the board to prevent shorting to adjacent traces. Solder the regulator leads.

( ) 34. Insert the 7805 regulator at the bottom of the heat sink. Attach securely with a 6-32x5/16" machine screw from the component side and a #6 lockwasher and nut on the solder side. Ensure that the heat sink is positioned with its sides parallel to the sides of the board to prevent shorting to adjacent traces. Solder the regulator leads.

( ) 35. Insert a 6-32x¼" screw through the 7905 regulator and mount the combination at the indicated location with a #6 lockwasher and nut. No heat sink is needed for this regulator. Solder the leads.

( ) 36. Mount the two .040 pin sockets for PI and PO as shown in the photo. Use cut resistor leads formed in a "U" and pulled down through the pair of holes to sit snugly on the sockets in order to hold them in place for soldering. Take care not to let the solder flow into the opening of the pin sockets.

( ) 37. Insert the 8080A microprocessor into the 40 pin socket at location A7. Ensure that Pin 1 is oriented properly.

( ) 38. Insert the 8228 IC into the 28 pin socket at location A9 as shown on the Assembly Diagram.

( ) 39. Insert the EPROM(s) into the 24 pin socket(s) at location(s) A10 (0000) and/or A11 (0400).

( ) 40. Insert the 16 pin header into the socket at location C3. See the User Guide for address selection information.

USER GUIDE----------

The IMSAI Interface Master Board (IFM) is a complete 8080A based microcomputer, configured as an intelligent interface controller. It is used in a number of IMSAI peripheral products, such as the IMSAI Floppy Disk System and the IMSAI Line Printer. The design of the IFM makes it adaptable to a wide variety of interface applications. Depending on the particular interface requirements, additional interface electronics may, or may not, be required.

PORT ADDRESSING

The address of the Command Output Port must be selected by jumpers (or a DIP switch) in position C3. Socket pins 1 through 8 correspond to Address Bits A0 through A7 respectively. Pins 9-16 provide for ground connections.

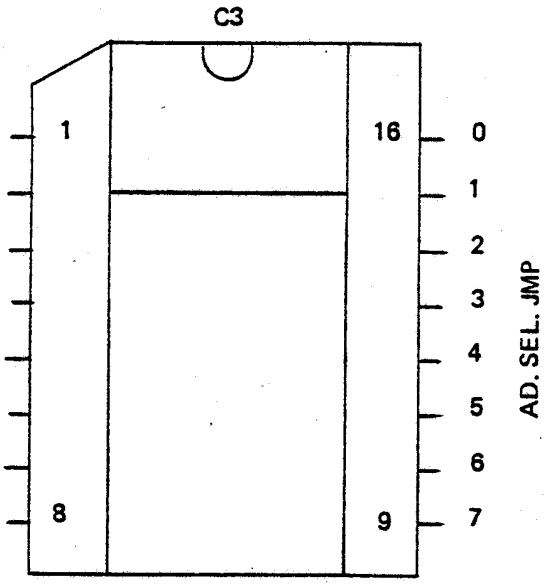
The address is selected as follows. For each Address bit which is to be a "0", the pin corresponding to that Address bit must be jumpered to ground. If a "1" is desired in any bit position, the corresponding jumper position is left open.

For example, to select address FD Hex, pin 2 is connected to ground pin 15. Pins 1, 3, 4, 5, 6, 7 and 8 are left open. To select address F6 Hex, pins 1 and 4 are connected to ground pins 16 and 13. Pins 2, 3, 5, 6, 7 and 8 are left open. FD is the IMSAI standard port address for floppy disks, and F6 is used for the Line Printer. Figure 1 depicts these connections.

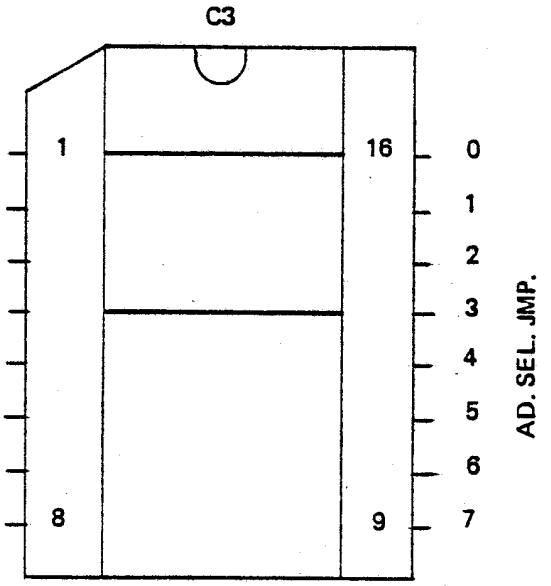
DMA PRIORITY

When multiple DMA channels are used in an IMSAI 8080 System, they are usually serviced on a first-come, first-served basis. When coincident DMA requests occur, priority is resolved using a daisy chain technique. To implement this, the Priority Output, (PO), of one IFM Board is connected to the Priority Input, (PI), of the IFM

Figure 1



JUMPERS SHOWN SET FOR FD
(IMSAI STANDARD ADDRESS FOR FLOPPY DISK)



JUMPERS SHOWN SET FOR F6
(IMSAI STANDARD ADDRESS FOR LINE PRINTER)

Board with the next lower priority. When using multiple IFM controllers, care must be taken when putting the SMPU into a Hold State for the duration of a block transfer of data, as all other controllers, regardless of priority, will be locked out for the duration of the transfer. Figure 2 depicts the DMA Priority connections for a Floppy Disk controller and a Line Printer controller.

EXTERNAL INTERFACE CONNECTIONS

All External Interface Connections are made via the 50 pin edge connector, J2, at the top of the IFM Board. Refer to Table 2 for a list of signals available and the corresponding pin assignments.

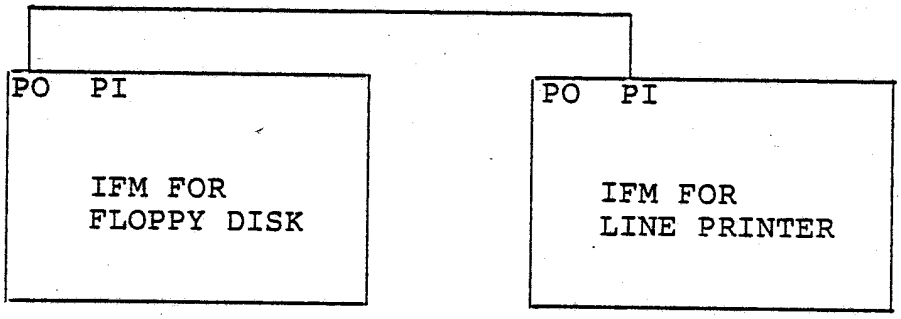


FIGURE 2. DMA Priority Set For: 1.Floppy Disk
2.Line Printer

J2 SIGNAL DEFINITIONS

PIN	SIGNAL NAME		PIN	SIGNAL NAME
1	RESET		2	/E7
3	/RESET		4	/E6
5	$T\emptyset_2$		6	/E5
7	RDYIN		8	/E4
9	MA10		10	/E8
11	MA11		12	MA14
13	MA13		14	MA12
15	MA15		16	MA9
17	MA8		18	INTE
19	WAIT		20	SYNC
21	MEMRW		22	INT
23	NC		24	HOLD
25	-5V		26	/INTA
27	DMA15		28	/MEMR
29	NC		30	/MEMRW
31	DISBUS		32	PADDR
33	DB0		34	MA7
35	DB1		36	MA6
37	DB2		38	MA5
39	DB3		40	MA4
41	DB4		42	MA3
43	DB5		44	MA2
45	DB6		46	MA1
47	DB7		48	MA0
49	+5V		50	+5V

TABLE 2. J2 SIGNAL DEFINITIONS

PROGRAMMING

The Control Program (Firmware) for the IFM Processor normally resides in the PROMs or ROMs at the Board locations A10 and A11. Only the programming considerations peculiar to the IFM will be covered in this document. Programming of 8080 based systems is covered in detail in the Intel 8080 Microcomputer Systems User's Manual.

IFM I/O The IFM communicates with the SMPU via a DMA Channel and a Single Byte Command Command Port. As viewed from the IFM's CPU, all IFM Input/Output is Memory Mapped. (Table 3). Input and output instructions DB Hex and D3 Hex must not be used in the IFM's Firmware, or System malfunction will result.

COMMAND PORT As viewed from the SMPU, the Command Port is an isolated output port whose address can be selected on the IFM Board. The address may range from 0 to 255 Decimal. When the SMPU outputs a byte to the Command Port, the IFM places the SMPU into a Hold State until it is ready to accept another command byte. This simplifies SMPU software requirements, as no additional data transfer synchronization (e.g. status bit) is required. A sequence of commands may be programmed as an inline string of output instructions.

As viewed from the IFM CPU, the single byte command port consists of a memory mapped status input port (address 1800H), and a memory mapped data input port (address 1400H). When a byte has been output by the SMPU, bit 0 of the status input port goes high and remains high until the command byte is input by the IFM. Bits 1 through 7 of the status port are not used and their states are indeterminate.

DMA CHANNEL The DMA Channel normally accesses the lower 32K bytes of the SMPU's memory by a virtual extension of the upper 32K bytes of the IFM's memory. For example, an IFM memory write operation to IFM address 8100H will result in a DMA write operation into the SMPU memory address 0100H. An IFM memory read operation from IFM address 92FFH will result in a DMA read operation from the SMPU memory address 12FFH.

The SMPU address is always the same as the IFM address, except for address bit 15. Bit 15 is normally forced to zero during the virtual memory extension as described. However, a peripheral board (such as the FIB or LIB) can force bit 15 to a one for a virtual extension of IFM memory space to the upper 32K bytes of SMPU memory space.

EXTENDING THE HOLD STATE The DMA Channel is normally used for the high speed transfer of data between the SMPU and the IFM using the cycle stealing technique. The SMPU is placed in a Hold State only long enough to transfer one byte of data. Between transfers the SMPU functions normally and can continue executing its own programming.

A certain amount of overhead time is involved in getting the SMPU into and out of the HOLD State. If desired, this overhead can be reduced while transferring long strings of data by placing the SMPU into a Hold State for the duration of the transfer. This is implemented by outputting a dummy command to the IFM after the DMA evolution has has begun. After the evolution, the dummy command is read by the IFM and the SMPU is released from holding. If the next desired command is known, it may be used in place of a dummy command. Note that once a command is output to the IFM command port, the SMPU remains in a Hold State until the IFM Processor reads the contents of the command port (1400H).

Since the DMA Channel is a virtual extension of the IFM's memory, it is possible for the IFM to execute program code stored in the SMPU's memory. Due to the overhead time involved, program execution will be slower. This technique can be used for firmware development, system troubleshooting, and special function routines which are not on the IFM PROMS.

IFM ADDRESS	SIGNAL
0000-07FF	EPROM (Firmware)
0800-09FF	RAM
0A00-0BFF	Not Available
0C00-0FFF	Available /E4 Decode
1000-13FF	Available /E5 Decode
1400	Command Data Port
1401-17FF	Not Available
1800	Command Status Port
1801-1BFF	Not Available
1C00-1FFF	Available /E8 Decode
2000-7FFF	Available No Decode
8000-FFFF	DMA

TABLE 3. IFM MEMORY MAP

FLOPPY DISK SYSTEM

CONTROLLER

FIB

14860 Wicks Boulevard
San Leandro, California 94577

FUNCTIONAL DESCRIPTION

The Floppy Interface Board (FIB) is used in conjunction with an IFM board to form a complete floppy controller. The Floppy Interface Board references the Mother Board Connector only to connect to an interrupt line and derive its voltage and ground from the proper pins.

Every effort has been made to keep the design simple and straight forward to maximize the reliability and ease of maintenance. MSI and LSI were used where appropriate and discrete components are held to a minimum for greater circuit reliability and ease of assembly.

The interface board works on a memory mapped basis and an 8205 three to eight line decoder is used to generate the proper command signals for the interface logic. All connections to the data bus are driven with tri-state drivers and all signals to the disk drives are driven with open collector drivers capable of sinking 40 milliamps. All lines from the disk drives are terminated with a resistor divider which is designed to match the impedance of the cable so there is no ringing effect on the signals. Two hex latches (74174's) are used to control the status information for the disk drive. These latches are loaded on output commands from the IFM board. There are also 2 24-pin, 8 bit shift registers used to accumulate the serial clock and data bits from the disk drives and to transmit them in a parallel mode to the microprocessor; or to receive a parallel load from the microprocessor and to transmit them serially to the disk. The write clock for the disk is derived by dividing down the 2 megahertz, phase 2 signal which comes from the MPU-A board using a 74LS193 counting chip. Finally, the determination of when a byte has been assembled is done by using a 74LS193 counting chip to count the 8 bits.

Unregulated plus 8 volts and ground must be supplied to the bus. On board regulation is used to arrive at the power supply levels needed to run the chips. Integrated Circuit power regulators with overload protection are used. The board is supplied with ample bypass filtering using both disk ceramic and tantalum capacitors.

The board connector which plugs into the Mother Board is a 100 pin edge connector on a .125 inch centers, 50 pins on each side. There is also a 50 pin edge connector on the right top of the board which is used to interconnect with the IFM board via a cable. This connector is on 0.10" centers. There is also a 26 pin edge connector on the same centers which is used to connect the Floppy Interface Board with the floppy disk drive in a daisy chain manner. The cable used is a terminated ribbon cable with a ground on pin 1. Overall board dimensions are 5" x 10" using two sided glass reinforced epoxy laminated with plated feed through holes to eliminate the need for any circuit jumpers. The contact fingers are gold plated over nickle for reliable contact and long life. All other circuitry is tin-lead plated for better appearance and more reliable solder connections.

Power On reset is used on this board to clear the disk control registers whenever the power comes up to the floppy controller. This will inhibit any inadvertent damage or writing on diskettes during a power up sequence, (i.e., when the floppy controller has not had power to it but the disk drives have has power applied to them). The power on sequence is performed in the IFM board whenever a reset has occurred.

FIB: THEORY OF OPERATION

INTERNAL ADDRESS DECODING

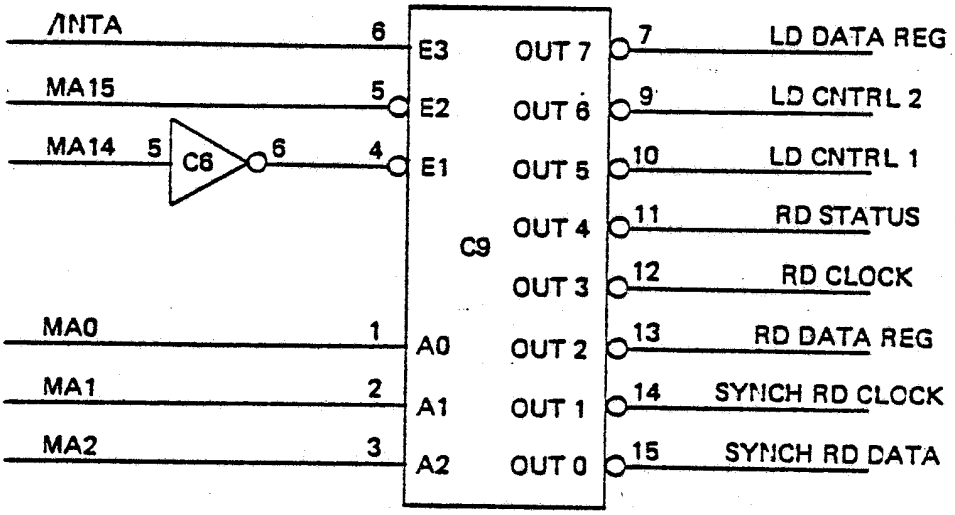


FIGURE 1
INTERNAL ADDRESS DECODING

All major functions on the FIB board are controlled from the IFM processor via a memory-mapped I/O technique. Address decoding is achieved through the use of the 8205 in position C9.

The 8205 is enabled when MA15 is low and MA14 is high. It may be disabled when INTA goes low.

Once C9 is enabled, MA0 - MA2 are decoded to produce a one of eight select function. The function of each select line is given below.

MA0 - MA15 = 4000: SYNCH ON READ DATA

This command is used to tell the floppy interface to go into a synchronization mode. The interface will then issue a HOLD command to the microprocessor until it has shifted a clock pattern into the shift register which has bit 5 missing. Note that the input data to the shift register is complemented, so this actually looks like bit 5 of the 74198 is a one.

When this bit becomes a 1, it says that the clock byte is missing a bit in this position. All missing clock patterns of significance in the 3740 have this bit as the first missing clock bit. Once this bit is detected, the microprocessor is allowed to read first the data and then the clock shift registers.

The firmware then compares them in order to determine whether or not this is the proper address and address and clock byte.

The read for this must be done with a 2 byte memory reference instruction to ensure the rapid timing between reading of the data byte and the clock byte (LHLD). This will result in the clock byte being read 2.5 microseconds after the data byte.

Since in a double density disk drive this would be longer than the next bit time, the clock register is inhibited from shifting during the time that we are waiting to read this clock byte. This is accomplished by pulling the mode control to 0 on the 74198.

MA0 - MA15 = 4001: SYNCH READ CLOCK

This is the Synch Read Clock Command. This command, as mentioned above, should be generated by referencing a Sync Read Data address (4000) with a two byte instruction (LHLD). When this command is operational, it gates the clock shift register onto the data bus through the 8T98 tri-state drivers. Note that inverting drivers are used because the clock and data registers both shift in the complement of the data.

MA0 - MA15 = 4002: READ DATA REGISTER

MA0 - MA15 = 4003: READ CLOCK REGISTER

These two commands operate in the same mode as the 4000 and 4001 commands with the following exception. When an input from the data register is to be accomplished, then the microprocessor must be held in a WAIT state until 8 bits have been assembled so that there is a complete byte.

This differs from the SYNCH READ CLOCK and SYNCH READ DATA commands where we are waiting to synch on a clock pattern. Once we have received the 8 bit byte, the data from the shift register is gated onto the data bus using the inverting tri-state drivers, and the microprocessor is taken out of the HOLD state.

Note that the single reference to the read data register will cause the data register to be transmitted. Only the read data operation may be used when attempting to read data from a floppy disk which has a bit time faster than 2.5 microseconds since, otherwise, the clock register will become out of synch.

MA0 - MA15 = 4004: READ STATUS

This command causes the contents of the disk drive status to be gated into the microprocessor. The sector input pulse is input to the microprocessor even though it is not used elsewhere in the design. It could be used at some later time to initiate a firmware system which works with a hard sectored disk as opposed to the IBM electronically sectored disk.

MA0 - MA15 = 4005: LOAD CONTROL 1

This command causes the content of the data bus to be transferred to the lower half of the floppy disk control register. The gating of these signals can then be controlled by the microprocessor to select a disk drive, to load the head on that drive, and to indicate to that drive when it is above track 43.

MA0 - MA15 = 4006: LOAD CONTROL 2

This command causes the contents of the data bus to be transferred to the upper half of the control register. It is used to initiate or generate seeks on the disk drive, to put the drive in the WRITE ENABLED mode, and to synch the PLO on the drive.

The command also sets a flip-flop which forces clock bits of all ones and data bits of all zeros to be written for one byte. This feature is used to initialize the WRITE logic when the WRITE ENABLE is first turned on. After this time, the controlling of logic is by the load data register command. The command is also used to clear the index pulse holding flip-flop whenever it is issued with DB07 a one.

The top two bits of this register are used to enhance the communication between the IFM and MPU memory. The firmware gets the value for this bit from the memory locations (bit 15) called out by the command strings and then forces bit 15 to be a one for internal operations so the DMA will function properly.

The second bit is used as an interrupt request bit and can be jumpered to any of the eight lines used as interrupt request inputs for the FIB. This bit is set whenever a command string execution has been completed (i.e., when the status byte value is modified from zero). It is cleared whenever a command is accepted from the MPU. Note that any command not defined is treated as a NOOP command and may be used to clear this bit.

MA0 - MA15 = 4007: LOAD DATA REGISTER

Load Data Register commands will transfer the contents of the data bus to the parallel shift register. The clock register is also loaded on this command with a value of FF, EF, D6 or C7 for memory address bits 3 and 4 equal to 00, 01, 10 or 11 respectively.

CONTROL OF IFM READY LINE

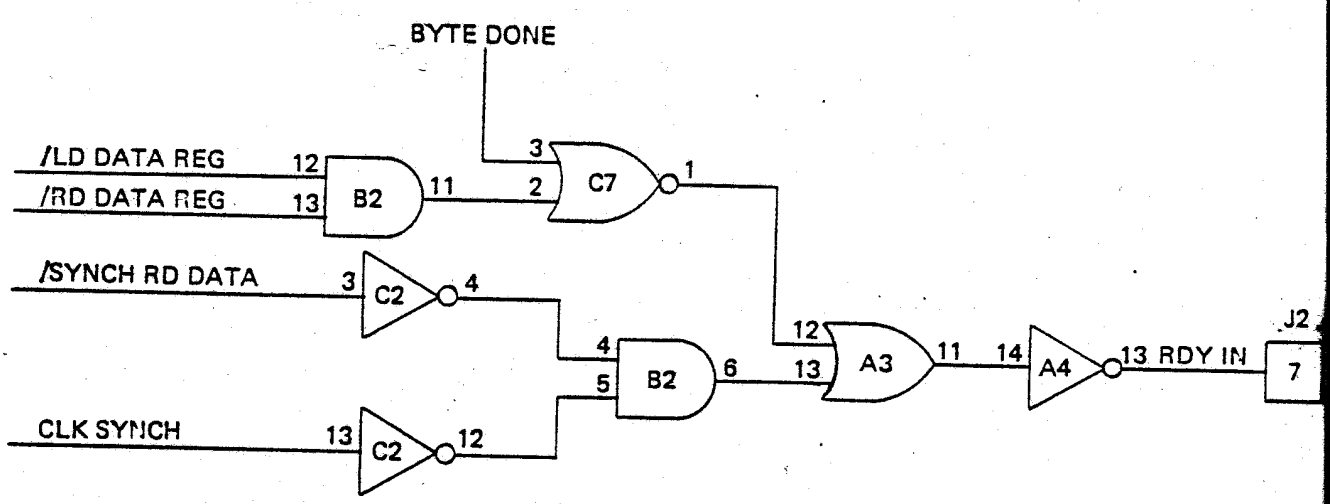


FIGURE 2
CONTROL OF IFM READY LINE

If a SYNCH READ DATA COMMAND (4000) is issued to the FIB board, the output of the AND gate at B2 - 6 will go high. This high level signal is inverted at A4 - 13, lowering the IFM READY line.

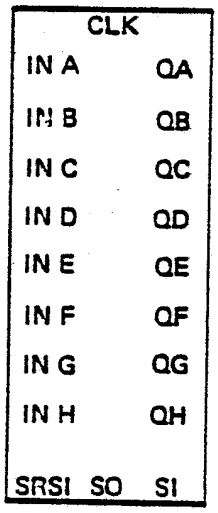
The IFM processor remains in a WAIT state until CLK SYNC appears high at C2 - 13. CLK SYNC goes high when a missing clock pulse is detected in bit position 5 of the clock shift register. This causes the output of the AND gate B2 - 6 to fall and the READY line to rise.

If either a READ DATA REF (4002) or LD DATA REG (4007) command is issued to the FIB board, the output of the OR gate at A3 - 11 will go high. This gets inverted at A4 - 13, and the IFM READY line is lowered.

The IFM processor will remain in the WAIT state until the BYTE DONE signal appears high at C7 - 3. The BYTE DONE signal becomes active when an 8 bit byte has been assembled in the shift registers (for a read) or 8 bits have output (written) to the disk.

The appearance of an active BYTE DONE signal causes the output of the OR gate A3 - 11 to fall. After inversion at A4 - 13, the READY line is raised, allowing the IFM processor to enter the RUN state.

THE 74198



SO	SI	FUNCTION
1	1	PARALLEL LOAD OUTPUTS = PARALLEL INPUTS ON RISING EDGE OF CLOCK
1	0	SHIFT RIGHT ON RISING EDGE OF CLOCK – $Q_{n+1} = Q_n / Q_A = SRSI$
0	0	DATA IS STABLE AT OUTPUTS QA – QH

FIGURE 3
THE 74198

The 74198 is a serial/parallel load shift register. This chip is used to assemble and transmit both the data and clock pulses used by the floppy disk. The functions used are shown in figure 3.

CLOCK SHIFT REGISTER

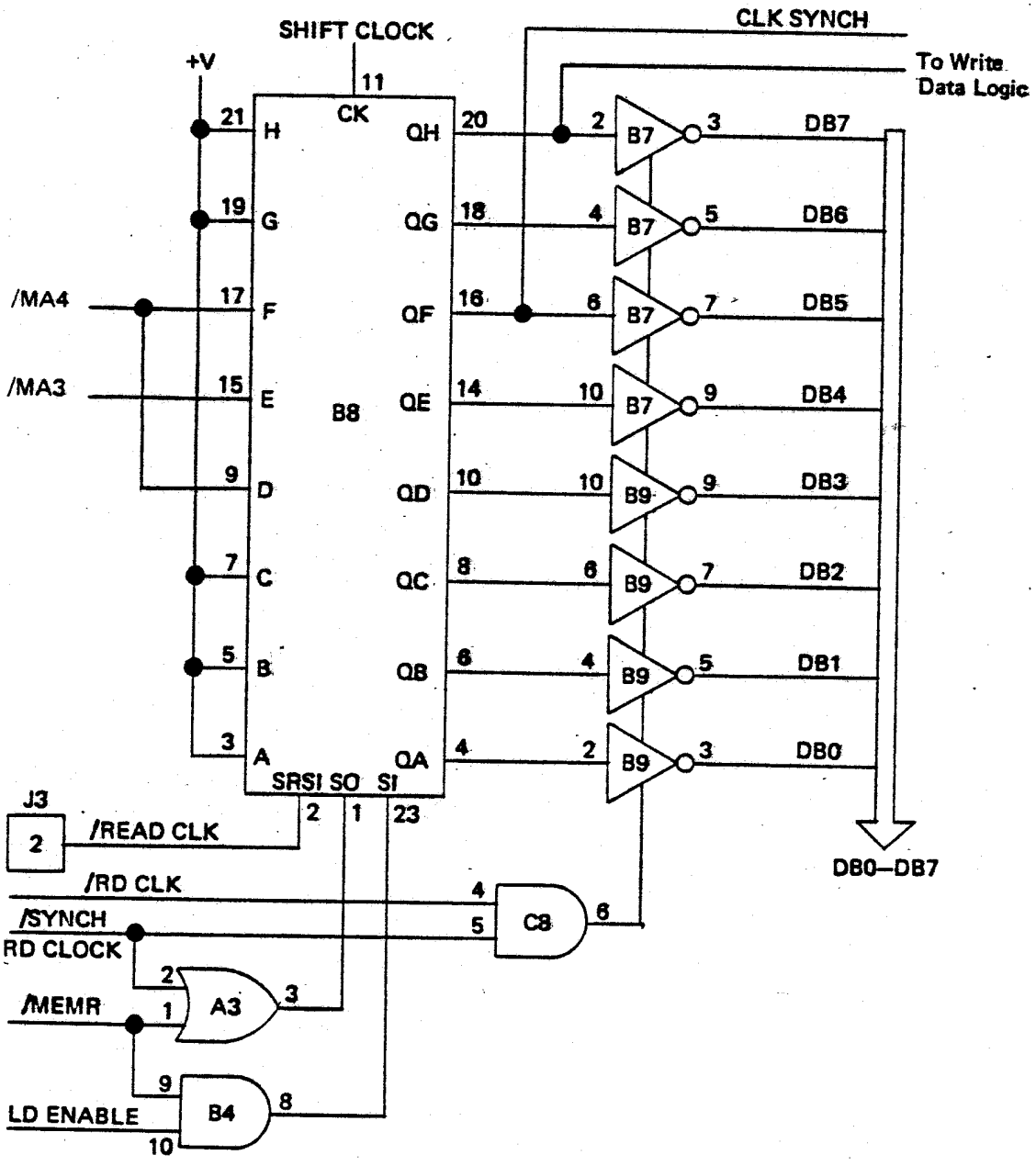


FIGURE 4
CLOCK SHIFT REGISTER

The 74198 in position B8 is used to output and input clock signals to or from the floppy disk.

READING THE CLOCK

A SYNC RD CLD (4001) command or a RD CLK (4003) command will output the 8 parallel bits of the 74198 at B8 onto the IFM Data Bus by driving the output of the AND gate at C8 - 6 low to enable the inverting drivers at B7 and B9.

NOTE: 8T98 inverting drivers are used since clock and data is input from the disk in inverted form.

Use of the SYNC RD CLK (4001) and RD CLK (4003) command assumes that an 8 bit word has been shifted into the clock shift register. These commands should only be used following a SYNC RD DATA command (4000) or RD DATA command (4002). To insure the proper timing of the read, only the LHLD instruction should be used to access the clock shift register.

SERIAL LOADING

The READ CLOCK line from the disk provides the serial input to the 74198 shift register. Clock data is input at the SRSI input to the 74198 and is shifted right on the positive edge of the shift clock.

WRITING CLOCKS

The shift register at B8 is also used in writing missing clock patterns to the disk. If a write to 4001, 4009, 4011 or 4019 occurs, one of four missing clock patterns is parallel loaded into the shift register.

A write to any one of these four addresses causes the S0 input of B8 to go high. When LOAD ENABLE goes high, the S1 input to B8 also goes high, and the shift register is loaded from the parallel inputs. MA3 and MA4 are used in writing missing clock pulses in positions D3, D4 and D5.

Once the parallel clock data is loaded, it is written to the disk. The serial output appears at the output Q_h of B8 and shifts right on the rising edge of the Shift Clock.

DATA SHIFT REGISTER

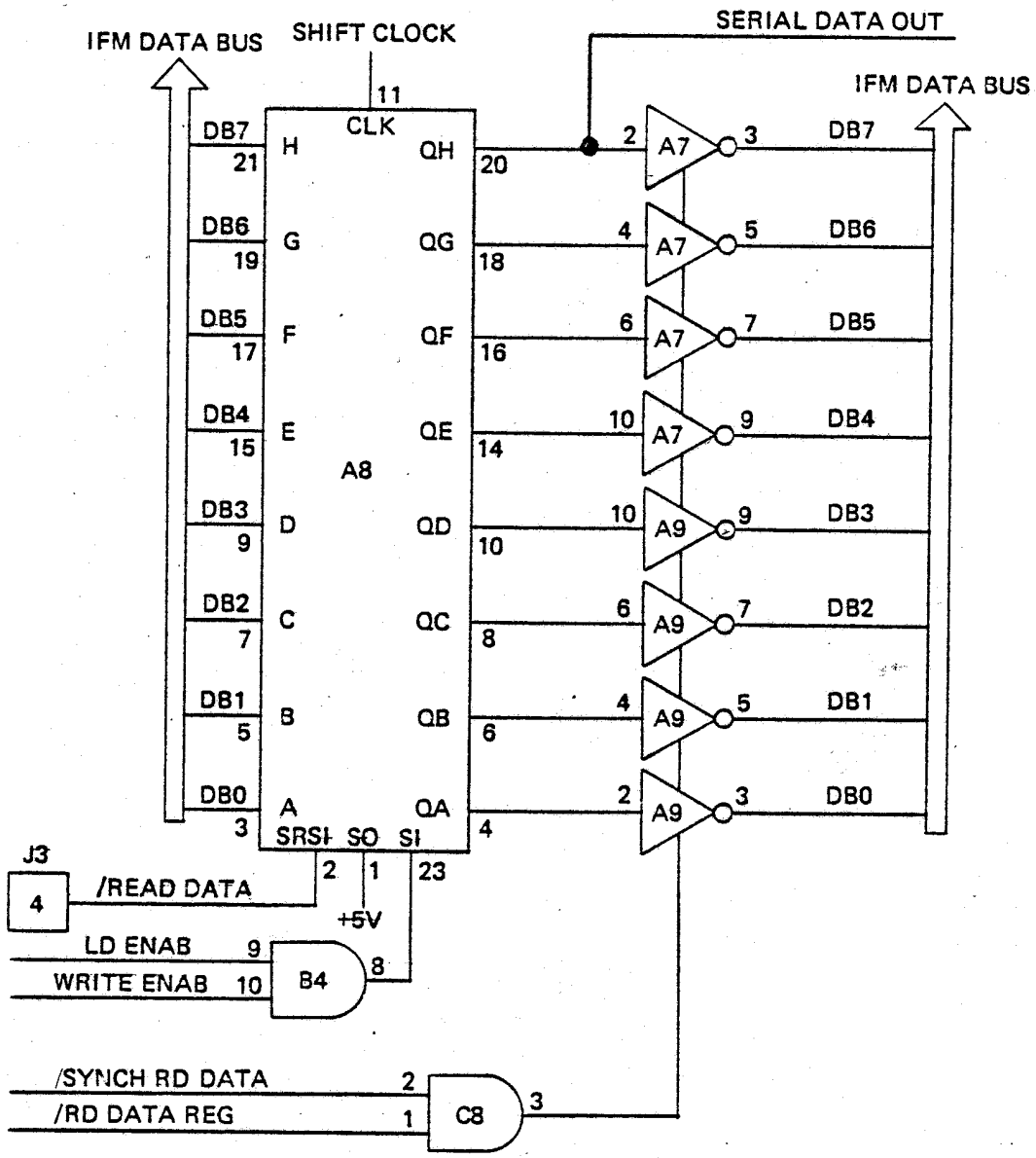


FIGURE 5
DATA SHIFT REGISTER

PARALLEL LOADING

If the WRITE ENABLE is set, the LD ENABLE signal will gate parallel data from the IFM Data Bus into the data shift register at A8.

Once the parallel data is loaded, it is written to the disk on the rising edge of the Shift Clock. Serial data output appears at Q_h of A8.

SERIAL LOADING

When the input S1 equals 0, serial data from the floppy disk is input to the shift register in inverted form at the SRSI input of A8 on the rising edge of the Shift Clock.

READING THE SHIFT REGISTER

If a $\overline{\text{SYNC RD DATA}}$ or $\overline{\text{READ DATA REG}}$ appears, the tri-state drivers at A7 and A9 are enabled. This allows the IFM processor to read the parallel outputs of the data shift register.

SYNCHRONIZATION

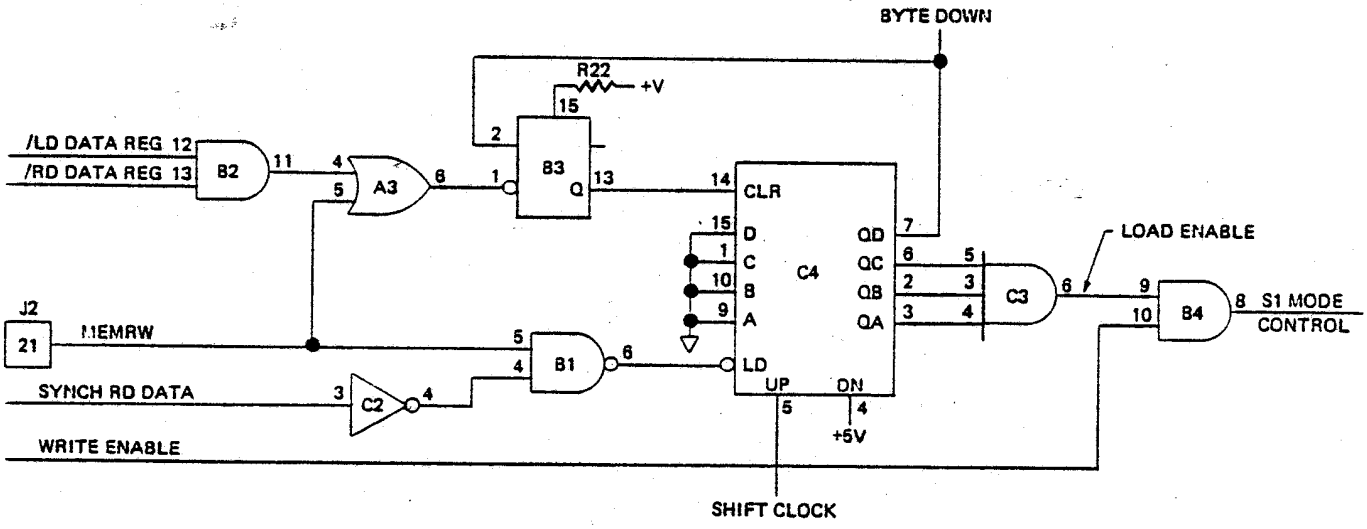


FIGURE 6
SYNCHRONIZATION

WRITE SYNCHRONIZATION

The $\overline{\text{LD DATA REG}}$ signal is used to load the data shift registers on a WRITE operation. The trailing edge of the $\overline{\text{LD DATA REG}}$ signal is used to fire the one-shot (B3) to clear the 4 bit counter (C4).

Count pulses are provided by the shift clock concurrent with clock and data pulses to/from the disk. At a count of seven, the LOAD ENABLE signal appears at the output of the AND gate C3 - 6. If the WRITE ENABLE is set, the S1 Mode Control signal goes high to allow parallel loading of the data and clock shift registers at B8 and A8 once the BYTE DONE signal appears.

At the count of 8, the Q_d output is used to generate the BYTE DONE signal indicating that an 8 bit byte has been output from the clock and data shift registers to the floppy disk.

READ SYNCHRONIZATION

When the $\overline{\text{SYNCH RD DATA}}$ line goes low, the counter at C4 is held clear. Once the IFM processor recognizes the missing clock pattern, SYNCH RD DATA will go high to enable the counter to start the count. Data is synchronized at this time.

The $\overline{\text{RD DATA REG}}$ line goes low, the IFM processor waits for the BYTE DONE before reading the 8 bits of data from the shift registers. Once RD DATA REG goes high, the one-shot at B3 is fired to clear the counter C4, and the count repeats itself for the next 8 bits read from the disk.

CLOCK W CLOCK/ DATA W CLOCK GENERATION

Both Write clocks are generated using the 4 bit counter at C5 to divide down the Ø2 clock. These two clocks are on opposite 2 microsecond clock intervals, and both clocks have a pulse width equal to the IFM Ø2 clock pulse width (275ns).

If the WRITE ENABLE is not set, both clocks are disabled since the LD input to the counter goes to zero and all outputs Q_a - Q_d go low.

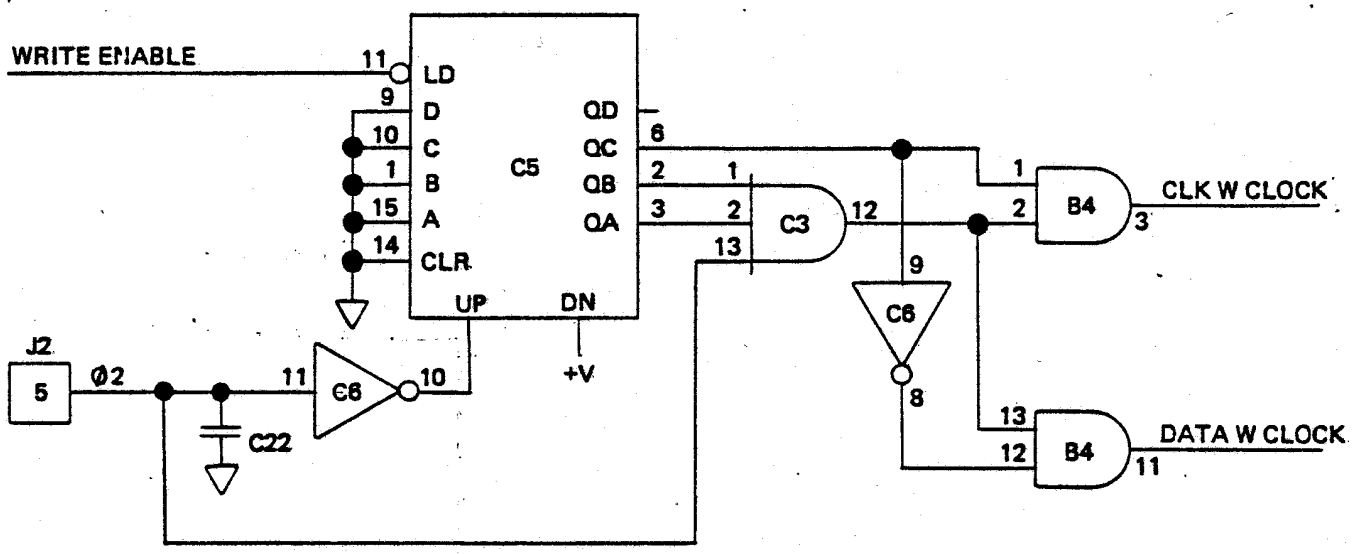


FIGURE 7
CLOCK W CLOCK/ DATA W CLOCK GENERATION

SHIFT CLOCK

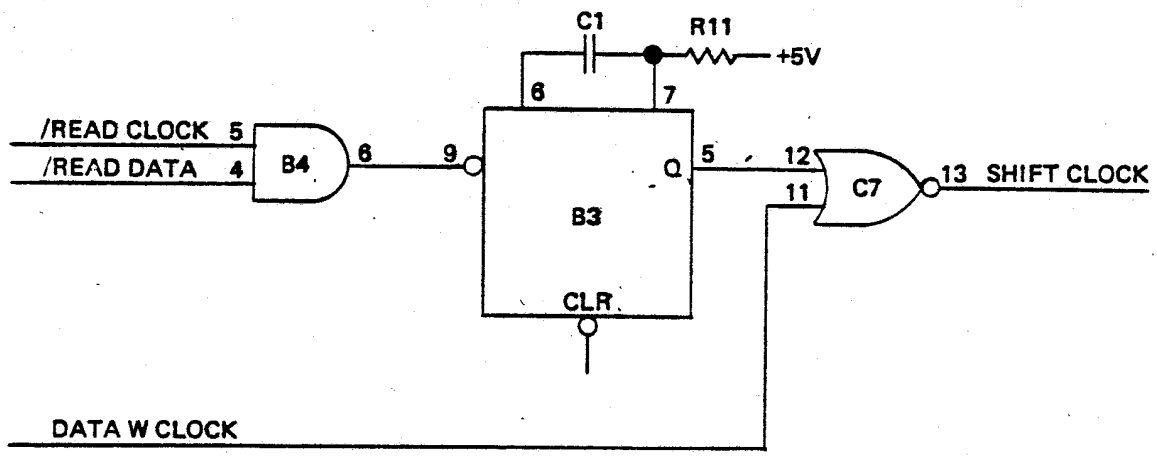
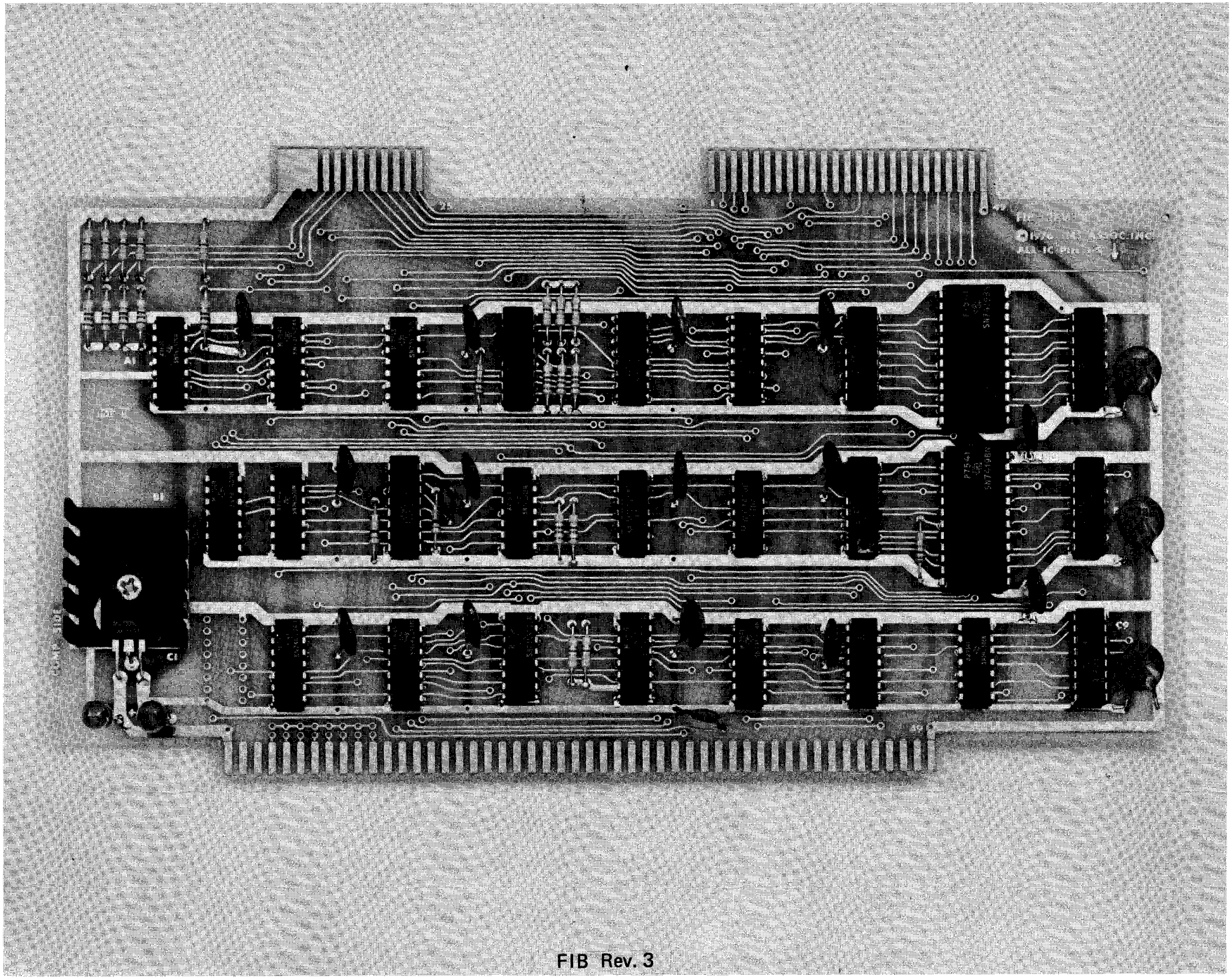
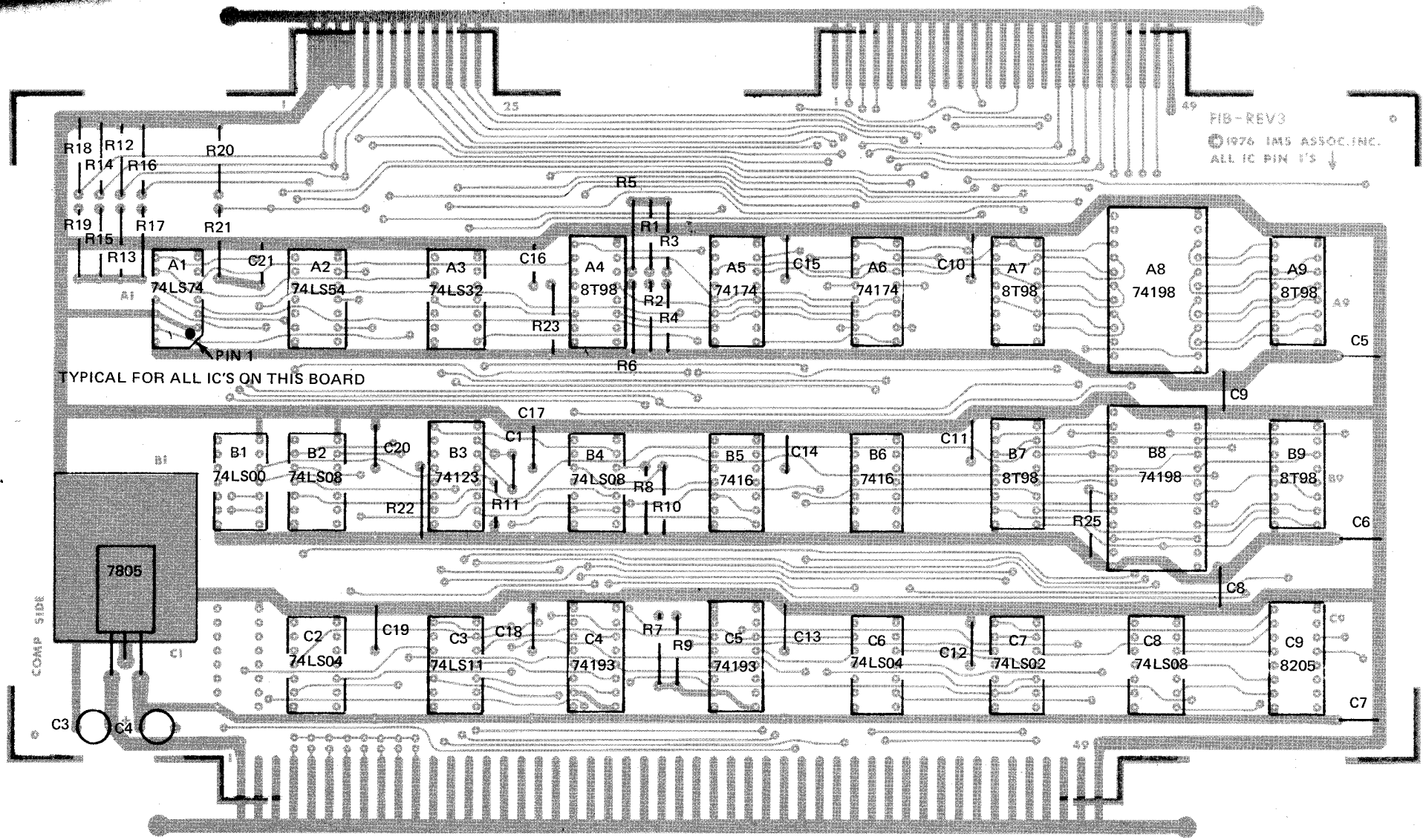


FIGURE 8
SHIFT CLOCK



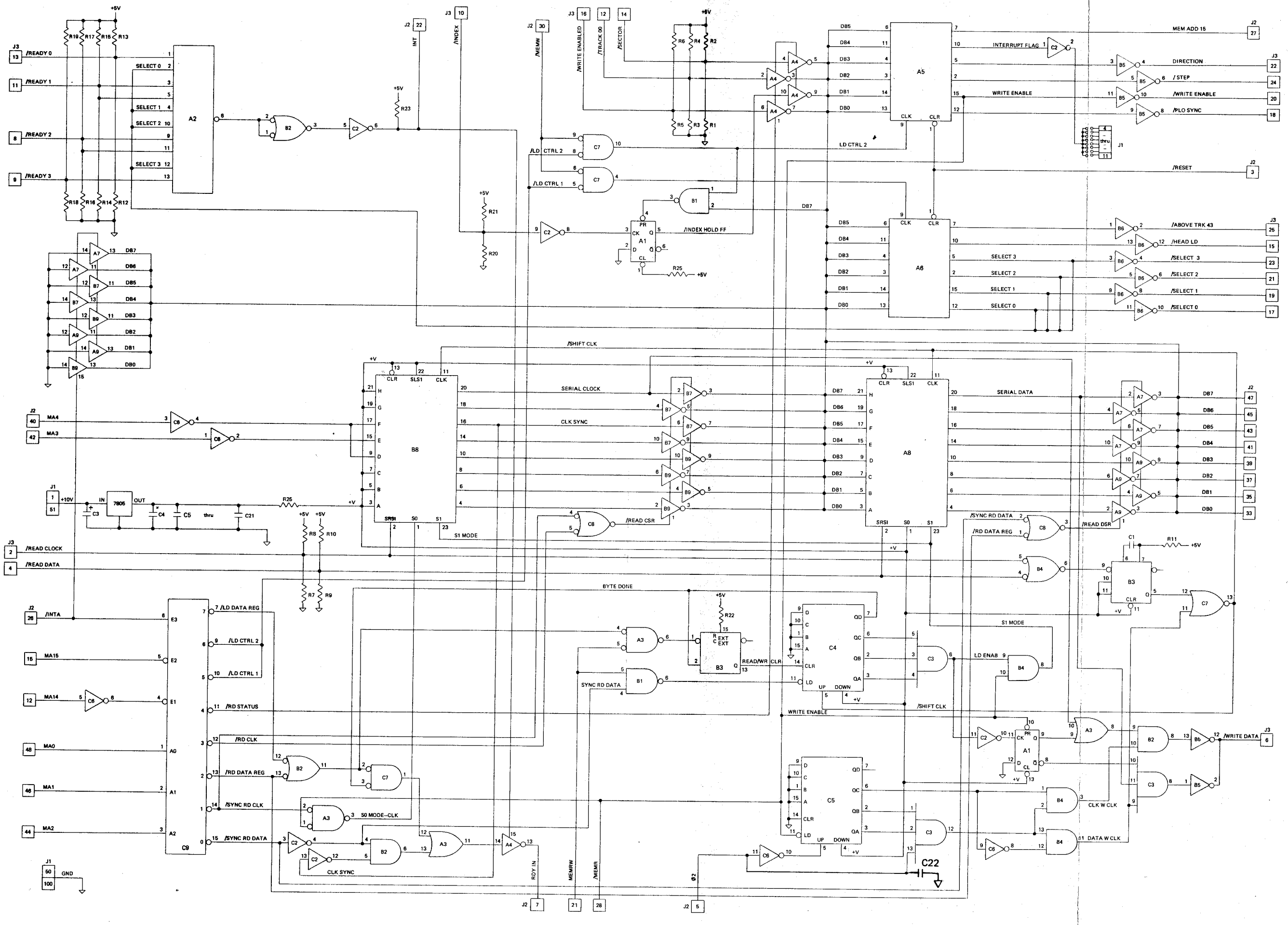
FIB Rev. 3



IMS ASSOCIATES INC.

ASSEMBLY DIAGRAM

FIB REV. 3 5/76



A1	74LS74
A2	74LS54
A3	74LS32
A4	8T98
A5 A6	74174
A7	8T98
A8	74198
A9	8T98
B1	74LS00
B2	74LS08
B3	74123
B4	74LS08
B5 B6	7416
B7	8T98
B8	74198
B9	8T98
C2	74LS04
C3	74LS11
C4 C5	74193
C6	74LS04
C7	74LS02
C8	74LS08
C9	8205
C1	47 pF
C3 C4	33uF
C5 thru C21	.1uF
C22	56pF
R1 R3 R5 R7 R9 R12 R14 R16 R18 R20	330 ¼W
R2 R4 R6 R8 R10 R13 R15 R17 R19 R21	220 ¼W
R11 R22	20K
R23 R25	1K ¼W

SCHEMATIC DIAGRAM
FIB REV. 3 5/76

BOARD: FIB

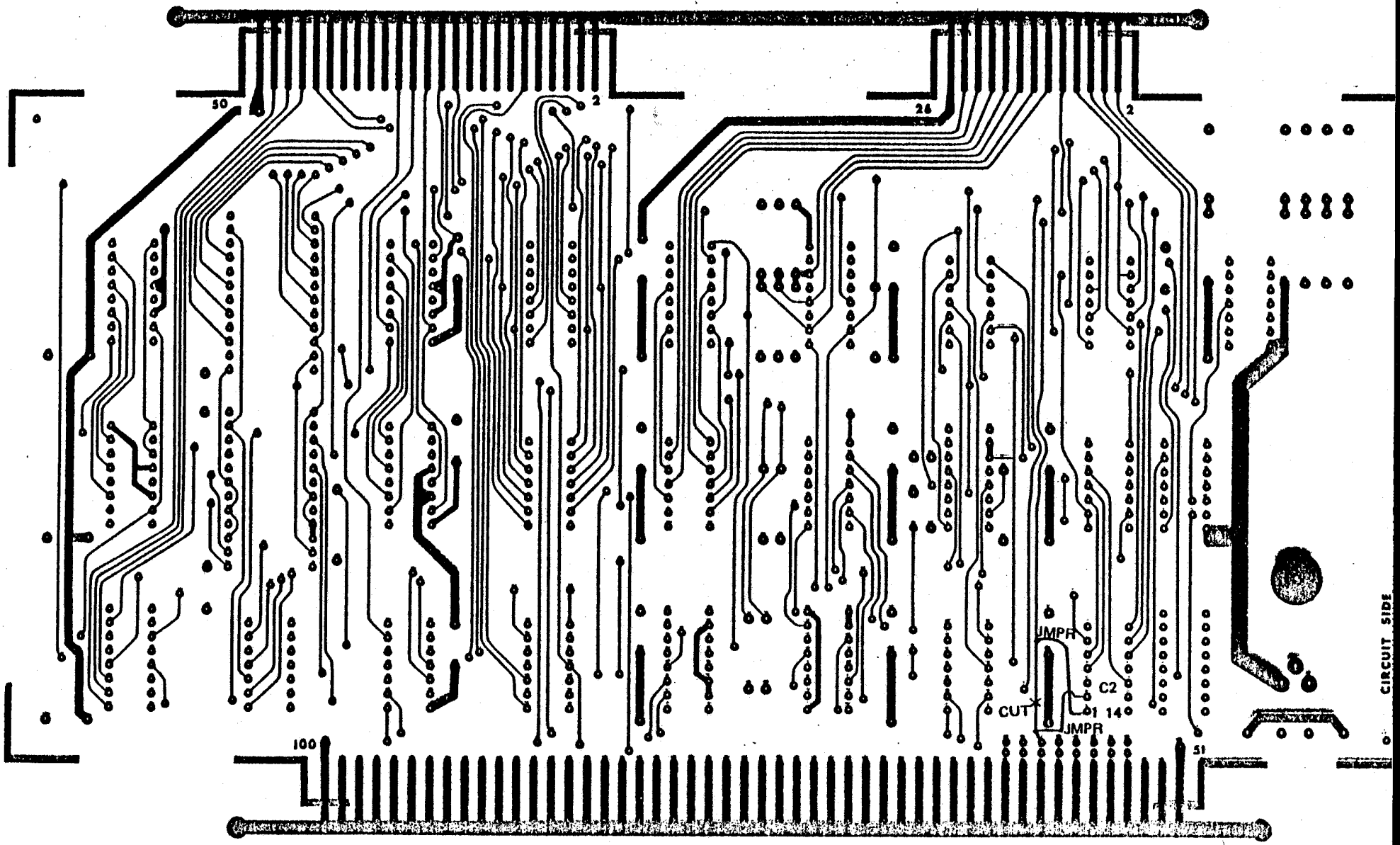
ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
74LS00	36-0740002	1	Quad 2 Input NAND (Low Power Schottky)/ SN74LS00N
74LS02	36-0740202	1	Quad 2 Input NOR (Low Power Schottky)/ SN74LS02N
74LS04	36-0740402	2	Hex Inverter (Low Power Schottky)/SN74LS04N
74LS11	36-0741101	1	Triple 3 Input AND (Low Power Schottky)/ SN74LS11n
74LS08	36-0740802	3	Quad 2 Input AND (Low Power Schottky)/ SN74LS08N
7416	36-0741601	2	Hex Inverter Driver Open Collector/SN7416N
74LS32	36-0743202	1	Quad 2 Input OR (Low Power Schottky)/ SN74LS32N
74LS54	36-0745401	1	2-2-2-2 Input AND-OR Invert (Low Power Schottky)/SN74SL54N
74LS74	36-0747402	1	Dual D Flip Flop Preset and Clear (Low Power Schottky)/SN74LS74N
74123	36-7412301	1	Dual Monostable Multivibrator, Retriggerable with Clear/SN74123N
74174	36-7417401	2	Hex D-Type Flip Flop with Clear/SN74174N
74193	36-7419301	2	Synchronous Up/Down 4-Bit Binary Counter/ SN74193N
74198	36-7419801	2	8-Bit Shift Register/SN74198N
8205	36-0820501	1	High Speed Binary Decoder/8205
8T98	36-0089801	5	Hex Tri-State Buffer
Capacitor	32-2010010	17	.luf Disk Ceramic Capacitor
Capacitor	32-0256010	1	56pf Disk Ceramic Capacitor
Capacitor	32-0247010	1	47pf Disk Ceramic Capacitor

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
Capacitor	32-2233070	2	33-25 Tantalum Capacitor
Heat Sink	16-0100002	1	Thermalloy/6106B-14
PC Board	92-0000020	1	Printed Circuit Board/FIB Rev. 3
Regulator	36-0780501	1	7805 5 Volt Positive Regulator
Resistor	30-3330362	10	330 Ohm, ¼ Watt/orange, orange, brown
Resistor	30-3220362	10	220 Ohm, ¼ Watt/red, red, brown
Resistor	30-4100362	2	1K Ohm, ¼ Watt/brown, black, red
Resistor	30-5200362	2	20K Ohm, ¼ Watt/red, black, orange
Screw	20-3402001	1	6-32x5/16"Phillips Pan Head Machine Screw
Nut	21-3120001	1	6-32 Hex Nut
Lockwasher	21-3350001	1	#6 Internal Star Lockwasher
Solder	15-0000001	5'	

FIB REVISION 3 BLUE WIRE CHANGES

INVERTS INTERRUPT SIGNAL

- Cut trace to Interrupt jumper pads (from A5 pin 10).
- Connect A5-10 side of cut to C2 pin 1.
- Connect C2-2 to Interrupt jumper pads.


50
2
26
2
100
51
JMPR
CUT
C2
1 14
JMPR
CIRCUIT SIDE

ASSEMBLY INSTRUCTIONS

1) Unpack your board and check all parts against the parts lists enclosed in the package.

2) If gold contacts on the edge connector appear to be tarnished, use pencil eraser to remove any oxidation. NOTE: Do not use Scotchbright or any abrasive material as it may remove the gold plating.

COMPONENT INSTALLATION

3) Insert and solder each of the ten 330 ohm ¼ watt resistors (orange/orange/brown) R1, R3, R5, R7, R9, R12, R14, R16, R18 and R20 as shown on the Assembly Diagram.

4) Insert and solder each of the ten 220 ohm ¼ watt resistors (red/red/brown) R2, R4, R6, R8, R10, R13, R15, R17, R19 and R21 as shown on the Assembly Diagram.

5) Insert and solder each of the two 20K ohm ¼ watt resistors (red/black/orange) R11 and R22 as shown on the Assembly Diagram.

6) Insert and solder each of the two 1K ohm ¼ watt resistors (brown/black/red) R23 and R25 as shown on the Assembly Diagram.

IC INSTALLATION

NOTE: All pin 1's point towards the lower right hand corner of the board.

7) Insert and solder one 74LS74 at location A1.

8) Insert and solder one 74LS54 at location A2.

9) Insert and solder one 74LS32 at location A3.

10) Insert and solder each of the five 8T98 ICs at locations A4, A7, A9, B7 and B9.

11) Insert and solder each of the two 74174 ICs at locations A5 and A6.

12) Insert and solder each of the two 74198 ICs (24 pin ICs. NOTE: If purchasing sockets separately, insert and solder sockets first.) at locations A8 and B8.

13) Insert and solder the one 74LS00 IC at location B1.

14) Insert and solder each of the three 74LS08 ICs at locations B2, B4 and C8.

15) Insert and solder the one 74123 IC at location B3.

16) Insert and solder each of the two 7416 ICs at locations B5 and B6.

17) Insert and solder each of the two 74LS04 ICs at locations C2 and C6.

18) Insert and solder the one 74LS11 IC at location C3.

19) Insert and solder each of the two 74193 ICs at locations C4 and C5.

20) Insert and solder one 74LS02 IC at location C7.

21) Insert and solder the one 8205 IC at location C9.

DISCRETE COMPONENT INSTALLATION

22) Insert and solder the seventeen .01 uF capacitors (C5-C21) as shown on the Assembly Diagram.

23) Insert and solder the two 33 uF tantalum capacitors (C3 and C4) as shown on the Assembly Diagram.

24) Insert and solder the one 47 pF capacitor (C1) as shown on the Assembly Diagram.

25) Insert and solder the one 56pF capacitor (C22) as shown on the Assembly Diagram.

REGULATOR AND HEAT SINK INSTALLATION

26) Bend the leads of the 7805 regulator at 90° angles approximately ¼" from the bottom edge of the regulator to facilitate insertion.

27) Insert the #6 screw through the 7805 regulator and heat sink on the component side of the board and attach with the washer and nut on the solder side of the board. NOTE: Be sure to hold the heat sink in proper vertical position while tightening the screw in order to prevent shorting to adjacent traces. Finally, solder the 7805 regulator to the board as shown on the Assembly Diagram.

FLOPPY DISK SYSTEM

CONTROLLER

FIB
FIRMWARE

14860 Wicks Boulevard
San Leandro, California 94577

FUNCTIONAL DESCRIPTION

The controller for the Floppy System is designed to make the operation as easy as possible for the end user. All power on initialization sequences and error recovery procedures are contained within the firmware in the floppy disk controller. Hence, if a hardware error is indicated by the floppy disk controller, it is an unrecoverable error and the user need not have error recovery procedures in his/her software. Similarly, the floppy controller is designed to monitor drives going NOT READY and becoming READY again, and to insure that proper head position is performed on these drives.

The communication between the master MPU and the IFM uses an output instruction (to a port address which has been selected on the floppy disk controller board) for passing single byte commands to the controller. The floppy disk controller has a DMA access to the master microprocessor's memory for retrieving string commands and transferring data and status back to the MPU. The two types of commands, (i.e., the single byte command, and the data string command) are described in more detail below.

The FIF board has provisions for using interrupts to assist the MPU program in determining when a command has been completed. The interrupt request line can be attached to any of the eight request lines for the PIB via a wired jumper. An interrupt request is generated whenever the processing of a command string is complete (i.e., the status byte is set non-zero). It is cleared whenever a command is accepted from the MPU via the output instruction. It should be noted that undefined commands are treated as NOT's and can be used to clear the interrupt request.

The master microprocessor is put into a wait state whenever it does an output instruction to the port of the floppy disk controller. It is held in this state until the floppy disk controller has taken the command from the master microprocessor and started processing it. The completion of an operation for single byte commands is signified by the IFM's ability to accept another command. The completion of a command string obtained from the MPU's memory is signified by the passing of a proper status word to the master microprocessor. Note that these command strings must always be in RAM memory since part of the command string is a location for the IFM to transmit back the status of the last operation.

THEORY OF OPERATION

FIF/IFM Firmware Description

This description will be divided into three separate sections. The first section will describe the major storage areas and the use of each area during the routine. The second section will give an individual description of frequently called subroutines. The third section will consist of a straight-line description of the code in the order that it is normally executed.

Part I Description of the Major Storage Areas

This description will consist of given the label used for the storage area in the program and then describing the use of this storage area.

PBAS

32 bytes in length and is used to contain the pointers to the address in main memory for retrieving command strings. These pointers are originally set to dummy values contained within the firmware and can be modified by the main program as described in the Users Guide.

PTRK

1 byte. Contains the physical track number that we are presently working on.

LTRK

1 byte. Contains the logical track number we are presently working on. Note that for normal operation the logical track number and physical track number will coincide. However, for strict IBM compatibility in the media readable format the logical track and physical track may differ if there are defective tracks on the disk.

SECT

1 byte. This byte contains the present sector we are working on, and has a value from 1 to 26. During the Read All routine it is used to contain the delay time before we start reading.

BUFA

2 bytes. This is the address pointer to the location in main memory where the data to be written on the floppy is contained or where the data read from the floppy is to be stored.

FUNC

1 byte. This byte in the four MSBs contains the function we are presently executing. This function is a number in the range is from 0 to 5. The fact that the logical track differs from the physical track has been removed prior to storing the general function in this byte.

INTF

1 byte. This is the interupt flag and controls whether the interupt routine returns a fatal error signifies that a drive is not ready. In all cases, except when we are testing for drive ready, the interupt flag has a value of 0 and this indicates that the drive was ready and has become not ready during an operation. This is a fatal error. In this case no retries are attempted.

RTRC

1 byte. This is the retry counter and is used for counting the number of attempts to do an operation when an error occurs. Ten attempts to retry an operation are made prior to telling the main program that an error has occurred.

STPT

2 bytes. This holds the address in main memory of the status byte. This byte is the second byte in all command strings.

HDFL

This byte contains the head flag to indicate to the firmware whether or not the head on the selected disk drive is lowered. If it contains a value of 0 the head is raised. If it contains a value of 1 the head has been lowered. During the time after an operation has been completed and prior to lifting of the head a value of 2 is put in this location and then after one revolution the head is raised.

DRVO

1 byte. This byte contains the present location of the head for drive 0. The most significant bit is the software write protect flag for this drive. If it is a 1, the drive is protected. A value is 7FH for the track location indicates that the drive should be restored over track 0 prior to any operation being performed.

This value is put into this location upon power up to indicate that all drives should be restored. It is also inserted whenever a drive is detected to be off line and should be restored over track 0 for alignment when it comes on line. It is also set when a track address error has occurred and we must restore to track 0 to attempt to relocate the desired track.

DRV1 1 byte. Refer to DRV0

DRV2 1 byte. Refer to DRV0.

DRV3 1 byte. Refer to DRV0.

TDRV

1 byte. This byte contains, in the four least significant bits, a select bit for the drive we are about to operate on. It is loaded by the drive address routine, DRAD and is references in the drive ready routine, DRDY when we are going to see if a selected drive is ready. The least significant bit corresponds to selecting drive 0 while bit 3 corresponds to selecting drive 3 and so forth.

SDRV

1 byte. This byte contains in the 4 least significant bits the select bit for the present drive.

DATB

133 bytes. This area is the data buffer location for the operating program. Note that the label is at the bottom of the stack so that data is pushed into this using the PUSH instruction during operation and popped off it during a write operation.

INTE

1 byte. This byte contains the present status of the interupt bit.

STAK

26 bytes. This is the stack area used for the program execution.

Description of the Frequently Called Subroutines

The format for this section is to give the four-letter name for the subroutine followed by a description of the operations performed within the subroutine.

DRAD

This is the drive address select routine. It operates by looking at the four least significant bits of the B register to determine what drive, if any, is selected. For the drive that is selected it sets that bit in TDRV and puts the address of DRV0 through DRV3, whichever is appropriate, in register pair H. Note that the routine can be called repetitively to perform operations on different drives.

Each time it sets up the address for a selected drive it clears the corresponding bit in the B register. Upon entry, if no drive is selected it returns with the 0 flag (Z) set. If any drive is selected it returns with Z = 0.

DRDY

This is the drive ready test routine. It tests the drive whose address is contained in register pair H to see if it is ready. Upon entry, it compares the value of TDRV and SDRV to see if the same drive is being reselected. If the same drive is being selected and the head on that drive is already lowered it does not reselect the head since this would be a duplicate operation. If either it is a different drive or the head has already been raised, the selected drive bit is set in control register 1. The interupts are then enabled follow by a SUB A register instruction. If, on the following instruction the A register has a value of 1 this indicates that the selected drive was not ready and the restore flag is set in its status location. The routine exits with the Z = 0 if the selected drive is not ready.

If the selected drive is ready, the routine checks to see if the restore flag for this drive is set. If it is, it checks to see if this drive is over track 0. If the drive is over track 0 it executes a step out to insure that the drive goes off track 0 and then steps back in to realign the track 0 position. If the drive is already off track 0 it attempts to move the head out until a track 0 indication occurs. If this indication does not occur within a maximum of 77 steps the drive is determined to be inoperable and a failure exit is taken. If the drive does go back over track 0 then the track address set to 0 and a successful exit is used.

LDHD

The load head routine is called when the formatter is going to perform the final step to reach the desired track. This routine loads the head and sets the greater than 43 bit if it is required.

CRCC Routine

This routine will compute the cyclic redundancy check bytes for data stored in a buffer location pointed to by register pair D, and for the number of bytes contained in register C. A complete description of the operation of this routine can be found in other INTEL publications.

HDRC

This routine computes the CRC for a address sector in the disk if calls the CRC routine with each byte as it would appear in the header sector and returns with the value of the CRC for this header in register pair H.

SYNC

This is the major routine used to find the desired sector on a track. Upon entry it calls HDRC to compute the expected CRC for this track. It then sets up in the registers the values of the track, sector, clock and address mark patterns so it can compare all of these within the time limit for each byte.

After the initial set up, the PLO is sunk and the routine goes into a wait pattern waiting for a clock byte which has bit 5 missing. Once this byte has been found the clock pattern and data pattern are read into register pair H. The clock pattern is compared first to see if it is appropriate. If it is not, the routine recycles and tries sinking the PLO again to obtain a new clock pattern. Each time the routine attempts to resink it checks to see if an index pulse has occurred. If two successive index pulses occur, it determines that it cannot sink properly on this track and indicates an error.

If the clock byte is correct, it does an increment on the data byte. (Note that the data byte should initially have a value of FE Hex and therefore 2 increments will cause it to be 0.) Next, it reads and compares the track address byte. If it is not equal a branch is made to determine whether or not the data byte was correct. If the data byte was not correct then it was a false sink and we attempt to resink. If the data byte was correct, then the track address we read was incorrect and we have a track address error which will cause us to restore the drive and reattempt the operation.

If the track address compares another increment is done on the data byte. This should set the 0 flag if the data byte was correct. Following this, the next byte is read from the disk. This byte should contain 0. After this is read the jump on whether or not the data byte of the ID mark was correct is performed. If it is correct, the CRC value is popped after the stack and the sector number is read and compared from the disc.

If it compares correctly, the second zero byte is read and ORed with the first 0 byte to ensure that they are both zero.

Then the first CRC byte is read and compared, and finally, the second CRC byte is read and compared. If both of these bytes compare, 10 more bytes are read to locate the head one byte from where the write enable should be turned on, or 2 bytes prior to where the PLO should be resunk for reading the data section of this sector. Following the reading of these 10 bytes the routine is exited.

RTRY

This routine is used to increment the retry counter. If 10 attempts have already been made to perform this operation, then an error is

taken. If not, the routine exits to its calling location where another attempt is made to perform the operation.

Straight Line Description of the Program

Prior to starting the main description, the interrupt processing routine will be described. The interrupt instruction used in the FIF is a RST 7 which causes an interrupt to location 38H. The interrupt routine looks at the intertupt flag. If it is 0, a selected drive has become not ready, and a fatal error is determined. No retries are are attempted because the drive or controller is obviously malfunctioning. A return is made to the main program through the error exit.

If the interrupt flag is a 1, it indicates that we are testing to see if the selected drive is ready, and the value of 1 is returned in register A to signify to the drive ready test routine that the selected drive is not ready.

On system power-up or RESET, the program sets the stack pointer and checks to see if drive Ø is ready. If it is ready, the program executes the bootstrap sequence as follows:

1. A JMP Ø instruction is DMA'd into system memory locations Ø, 1 and 2, so that the front panel operations RESET, EXAMINE Ø, and RUN cause the system processor to enter on infinite wait loop.

2. A small program to read sector 1 of track Ø from drive Ø is DMA'd into system memory starting at location 8Ø.

3. The low byte of the address in the JMP instruction is changed to cause the system processor to jump into the bootstrap code above location 8Ø.

If the drive is not ready, or when the bootstrap sequence is complete, the default pointers are set up. Once this is done, the software protect flag is turned on for all drives. No operation need be performed on the individual drives since this will be done by the scan loop while waiting for commands from the main processor. The scan loop actually has 2 separate sections. The first section is used when the head is down on a selected drive. This inhibits selecting of other drives since the head would be raised. We stay in this loop until two revolutions have occurred or another command request is received from the main processor. If two index pulses have occurred, the head on the selected drive is raised and the flags are set appropriately.

If the head was not down, we go into the section of the scan loop where we look at each drive. If a drive has become ready and a restore flag is set on it, then the restore is done on that drive. If a drive is ready and has been ready, no action is performed. If a drive becomes not ready, the restore flag is set on it. These operations are performed by calling the DRAD and DRDY subroutines. In either of these loops a check is made to see if the main program is requesting an action. If it is, a jump is immediately taken to location ACTN where the type of action requested is determined. An action code or 0 calls for a command string to be read from main memory and processed. This operation will be described in the next section.

An action code of 1 is the setting of a new address in main memory for a pointer. The address of the pointer is formed in subroutine PADO and then RBYT called to read the next two bytes from main processor and to store them into the proper pointer location.

An action code of 2 calls for a restore to be executed on all drives whose bit is set in the four least significant bits. Note that the subroutine DRAD is used to set the addresses for each of the bits and determine when all drives have been processed. For each selected drive, the flag is set in its respective status byte. The restore actually will be done in the scan loop at a later time.

An action code of 3 calls for the software write protected to be set in for each drive whose bit is set in the four least significant bits. Again, the same routine DRAD is used to cycle through the four least significant bits.

An action code of 5 calls for the software write protect bit to be cleared for each drive which is selected in the four least significant bits. If the action code is greater than 5, it is considered to be a NOP and the routine returns to the scan loop.

For an action code of 0, the address of the string in main memory is determined. Then the string is analyzed and as a function of the operation code the parameters are checked to ensure they have the proper value. This is done in a straight line fashion and the routine ends up at ACT6 with all of the parameters except for the separate logical track if it is a special IBM function. At this time, if it is a special IBM function, the logical track number is read and stored in LTRK after being parameter checked.

The drive is then checked to ensure that it is ready. If the drive is ready, and the write protect status is OK, the

drive is then positioned. Prior to positioning the drive, the retry counter and interrupt flags are set to 0 since any interrupt from now on will be a fatal error on the part of the drive. The difference between present track and the desired track is computed. If it is 0, we go out to test if the head is loaded. If the head is already loaded, then we may continue without any time delay. If the head has not been loaded, we then come back to the section of the routine where the track step delay is performed. Just prior to the last step for the correct track, the head is loaded. The 16 millisecond delay is used.

If this operation requires steps in or out, register E is set with the direction bit and the head is revised.

The program then issues a track to track step each 6 milliseconds until there is 1 track to go. At this time, the load head routine is called and after the 6 millisecond step delay, we go through a 10 millisecond head settling delay. At the completion of the drive positioning, we are now ready to accomplish whatever operation was called for in the action code. This occurs at ACTB where the function in four MSBs of FUNC is interpreted and we jump to the proper routine. The separate routines for processing will be described in each of the following paragraphs.

The read all routine, RALL, starts by setting for 64 bytes to be read. Note that the clock and data values are saved for each byte and this is 128 bytes to be transferred. After the set up, the routine waits until a index pulse has occurred and then delays for the proper number of milliseconds (0 to 255). After the delay, the PLO is sunk and the routine reads the clock and data pattern from 64 successive bytes storing them in the data buffer area DATB. Then the data buffer area is moved to the proper location in main memory and the stack pointer is reset to it's proper value. The routine then goes to the scan loop to wait for another operation.

WRIT

The write routine is used to write a sector of data onto the disk. The 128 bytes are first retrieved from the main memory. After this, the CRC is computed. Note that 129 bytes are used to compute the CRC since the value of the data in the Data Address Mark is used as the first byte for the CRC computation. This is stored in memory so it is readily available using pop instructions during the execution of the actual write on the disk. The sector location routine SYNC is then called to get in the proper position on the disk for writing the data in this sector.

SYNC exits after reading 10 trailing 0 bytes following the address header. The setup is then done for the write routine and the write enable is turned on at approximately the end of the 11th byte. At this time, the data loop starts by writing 6 bytes of zeros followed by the Data Address Mark, 128 bytes of data, the two CRC bytes and 1 trailing 0 byte. At this time, a successful write has been completed and the write enable is cleared. A normal return is taken.

WDSC

The next routine WDSC writes the Deleted Data Address Mark on an individual sector. It again starts by calling SYNC to find the proper sector on this track. Once SYNC exits, the set up is done in the registers to perform the write. A delay is executed prior to setting the write enable. This ensures that the 11th byte after the header will pass prior to the write enable being set. Once write enable is set, 6 bytes of zeros are written followed by the Deleted Data Address Mark and a trailing zero byte. At the completion of this byte, the write enable is cleared and a successful return is taken.

Read Routine

This routine is used both for the check read function and the read function. The difference being that after the data is read and the CRC is checked, for a Check Read the data is not moved back to the main memory.

The routine starts by calling the SYNC to position to the proper sector. After returning from SYNC, the parameters for checking the data address mark are put into the registers. A delay is then executed to ensure that the head has passed the area where the write current is turned on during a write operation before syncing the PLO. Then the PLO is sunk and the read routine goes into the wait mode waiting for the next byte with a missing clock pulse to occur. When this byte is received, both the clock and data from the byte are read into register pair H. First the clock byte is compared to ensure that it has the proper value (Hex C7). If this value is proper, the data byte is compared. If the data byte does not compare with the value for a normal sector (FEH), a branch is made to check to see if this is a Deleted Data sector (FBH). If a Deleted Data Address Mark has been found, there is a Deleted data read error and no retries are attempted, and an error exit is immediately taken. If it is neither a Data nor a Deleted Data Address Mark, it is an error and a retry is attempted.

After the data address mark has been successfully read, the routine reads 130 bytes. The first 128 of these are data and the last two are the CRC bytes. The interrupt is disabled after he CRC bytes. The CRC is then checked, a byte at a time. Note that the data pattern from the Data Address Mark is the first byte processed by the CRC routine. The 130 bytes are then processed and the result should be a 0 CRC value, if a proper read has been performed. If not, the CRC error is set and a retry attempt is made. If all the data is correct, the value in FUNC is checked to see if it is a check read or a read. If the function is a read, a jump is made to return the data to the main memory. If it is a check read, a normal return is made.

FRMT

This is the format routine which writes all the gaps and index marks on a track for later use by the read and write routines. Due to the time constraints during writing, the set up must be made for all variable parameters prior to initiating the formatting of a track. Hence, upon entry the format routine calculates the CRC value for each header for each sector to be written. This is done using the routine HDRC and the resulting values are stored in the data buffer area. Note that the CRC value for the data sectors is identical for all 26 sectors since they all have the same address mark, followed by 128 bytes of 0. Hence, this CRC is used as constant. Once the header CRC's have been computed, the routine does the set up for starting a write. Then it waits for the index mark at which time it is to start writing.

At this time, it sets the write enable and writes the last 46 bytes of GAP IV. Note that whenever a gap is written in this routine, the counter is always set to value one less than the size of the gap and then the final byte is written. The reason for this is to permit the maximum set up time for writing the next byte which is always a special clock pattern byte.

A sector consists of first writing GAP I which is 32 bytes in length. Note that in this case the counter is set to 30 since a single trailing 0 byte is written after the CRC value at the end of each sector. In the case of the first GAP I (prior to sector 1), the gap is only 31 bytes in length.

After writing GAP I, the Index Address Mark is written followed by the track number, a zero byte, the sector (contained in register B throughout the routine), another

zero byte, followed by the 2 CRC bytes (which have previously been stored in a data area). This is followed by GAP II which is 17 bytes in length. Hence, the counter is set to a value of 16. The end of GAP II is followed by the Data Address Mark and 128 bytes of zeros (the data field). The two CRC bytes, which are common for all data sectors, are then written followed by a trailing zero byte.

The sector number is checked to see if the format for 26 sectors has been written If not, a return is made to write the next sector. If the 26 sectors have been written, then the first section of GAP IV is written. This consists fo writing 0's until the index pulse occurs. At this time the write enable is cleared and a successful return to the main routine is taken.

```
                ;26 OCT 76. BRH. ADDED BOOTSTRAP LOADER.
                ;21 OCT 76. BRH. MERGED PROGRAM INTO ONE FILE.
                ;
                ; ********* FLOPPY INTERFACE FIRMWARE *********
                ;
                ; IFM RAM ADDRESSES
                ;
0800 =          PBAS    EQU     800H    ;RAM STORAGE FOR COMMAND POINTERS
0820 =          PTRK    EQU     PBAS+32 ;PHYSICAL TRACK NUMBER
0821 =          LTRK    EQU     PTRK+1  ;LOGICAL TRACK NUMBER
0822 =          SECT    EQU     LTRK+1  ;SECTOR NUMBER
0823 =          BUFA    EQU     SECT+1  ;ADDRESS OF BUFFER IN MAIN MEMORY
0825 =          FUNC    EQU     BUFA+2  ;PRESENT FUNCTION IN 4 MSB
0826 =          INTE    EQU     FUNC+1  ;INTERRUPT FLAG (LATCH CONTENTS)
0827 =          INTF    EQU     INTE+1  ;INTERRUPTS: 1 FOR TESTING DRIVE,
                                        ;  0 IF INTERRUPT IS FATAL ERROR
0828 =          RTRC    EQU     INTF+1  ;RETRY COUNTER FOR ERROR PROCESSING
0829 =          STPT    EQU     RTRC+1  ;HOLDS STATUS BYTE ADDRESS
082B =          HDFL    EQU     STPT+2  ;0 IF HEAD UP, 1 IF DOWN,
                                        ;  2 IF WAITING TO BE RAISED
082C =          DRV0    EQU     HDFL+1  ;DRIVE TRACK LOCATION IN 7 LSB.
082D =          DRV1    EQU     DRV0+1  ;  MSB IS 1 IF DRIVE IS SOFTWARE
082E =          DRV2    EQU     DRV1+1  ;  WRITE PROTECTED.  7 LSB = 7F
082F =          DRV3    EQU     DRV2+1  ;  IF DRIVE MUST BE RESTORED.
0830 =          TDRV    EQU     DRV3+1  ;DRIVE SELECT BIT FOR NEXT DRIVE
0831 =          SDRV    EQU     TDRV+1  ;DRIVE SELECT BIT FOR THIS DRIVE
08B6 =          DATB    EQU     SDRV+133 ;TOP OF 133 BYTE DATA BUFFER
0900 =          STAK    EQU     900H    ;TOP OF STACK
0900 =          RAM     EQU     900H    ;START OF DEBUG RAM
                ;
                ; POWER UP ROUTINE
                ;
0000                    ORG     0
0000 310009             LXI     SP,STAK ;SET STACK POINTER
0003 97                 SUB     A       ;SET PARAMS FOR DRDY...
0004 322C08             STA     DRV0
0007 323108             STA     SDRV
000A 0601               MVI     B,1     ;FORM DRIVE 0 ADDRESS...
000C CDBD02             CALL    DRAD
000F CDE302             CALL    DRDY    ;CHECK TO SEE IF DRIVE 0 IS READY
0012 C28100             JNZ     SCLPH   ;SKIP BOOTSTRAP IF NOT READY
0015 97                 SUB     A       ;RESET SYSTEM MEMORY BIT...
0016 320640             STA     4006H
0019 67                 MOV     H,A     ;ZERO HL...
001A 6F                 MOV     L,A
001B 3EC3               MVI     A,0C3H  ;GET JUMP OPCODE
001D 320080             STA     8000H   ;STORE AT 0 IN SYSTEM MEMORY
0020 220180             SHLD    8001H   ;STORE ADDRESS TO JUMP TO
0023 218080             LXI     H,8080H ;START OF BOOT CODE IN SYSTEM
0026 114200             LXI     D,SYSCM ;POINTER TO BOOT CODE IN PROM
0029 0E1F               MVI     C,SYSLN ;LENGTH OF BOOT CODE
002B CD9103             CALL    DMOV    ;TRANSFER CODE TO SYSTEM MEMORY
002E 3E87               MVI     A,SYSTR ;POP IN LO BYTE OF JUMP ADDRESS
0030 320180             STA     8001H   ;  SO SMPU JUMPS TO BOOT CODE
0033 C38100             JMP     SCLPH   ;CONTINUE AT SCAN LOOP HEADER
                ;
```

```
0038                    ORG   38H
0038 3A2708     INTR:   LDA   INTF
003B B7                 ORA     A
003C C0                 RNZ
003D 0E91               MVI   C,91H
003F C38302             JMP   AERX
                ;
                ; SYSTEM BOOT CODE
                ;
0042 21         SYSCM:  DB        21H       ;READ SECTOR COMMAND
0043 00         STATS:  DB        00H       ;STATUS BYTE
0044 00                 DB        00H       ;HI BYTE OF TRACK #
0045 00                 DB        00H       ;LO BYTE OF TRACK #
0046 01                 DB        01H       ;SECTOR #
0047 0000               DW        0000H     ;ADDRESS OF BUFFER
                ;
0049 97         START:  SUB       A         ;MAKE ZERO
004A 328100             STA       SYSTA     ;RESET STATUS BYTE
004D D3FD               OUT       0FDH      ;EXECUTE POINTER ZERO
004F 3A8100     STAR0:  LDA       SYSTA     ;GET STATUS BYTE
0052 B7                 ORA       A         ;IS IT 0?
0053 CA8D00             JZ        SYST0     ;LOOP AS LONG AS IT IS
0056 FE01               CPI       1         ;STATUS OKAY?
0058 CA0000             JZ        0         ;JUMP INTO BOOTSTRAP IF SO
005B 2F                 CMA                 ;PUT ERROR CODE IN LIGHTS...
005C D3FF               OUT       0FFH
005E C38700             JMP       SYSTR     ;TRY TO BOOT AGAIN
                ;
001F =          SYSLN   EQU       $-SYSCM
0081 =          SYSTA   EQU       STATS-SYSCM+80H
0087 =          SYSTR   EQU       START-SYSCM+80H
008D =          SYST0   EQU       STAR0-SYSCM+80H
                ;
                ; DEFAULT POINTERS
                ;
0061 8000       DEFP:   DW        00080H
0063 0010               DW        01000H
0065 0020               DW        02000H
0067 0030               DW        03000H
0069 0040               DW        04000H
006B 0050               DW        05000H
006D 0060               DW        06000H
006F 0070               DW        07000H
0071 0080               DW        08000H
0073 0090               DW        09000H
0075 00A0               DW        0A000H
0077 00B0               DW        0B000H
0079 00C0               DW        0C000H
007B 00D0               DW        0D000H
007D 00E0               DW        0E000H
007F 00F0               DW        0F000H
                ;
                ; SCAN LOOP HEADER
                ;
0081 210008     SCLPH:  LXI       H,PBAS    ;SET DEFAULT POINTERS...
0084 116100             LXI       D,DEFP
0087 0E20               MVI       C,32
0089 CD9103             CALL      DMOV
```

```
008C 97                 SUB     A       ;INITIALIZE VARIABLES...
008D 322B08             STA     HDFL
0090 322608             STA     INTE
0093 323108             STA     SDRV
0096 3E7F               MVI     A,7FH
0098 212C08             LXI     H,DRV0
009B 77                 MOV     M,A
009C 23                 INX     H
009D 77                 MOV     M,A
009E 23                 INX     H
009F 77                 MOV     M,A
00A0 23                 INX     H
00A1 77                 MOV     M,A
                ;
                ; MAIN SCAN LOOP
                ;
00A2 3A2B08     SCLP:   LDA     HDFL    ;GET HEAD FLAG
00A5 B7                 ORA     A
00A6 CAD300             JZ      SCL1    ;JUMP IF HEAD NOT DOWN
00A9 3A0018     SCL2:   LDA     1800H   ;DOWN, CHECK COMMAND
00AC 1F                 RAR
00AD DAE800             JC      ACTN
00B0 3A0440             LDA     4004H   ;NO, CHECK FOR INDEX
00B3 E602               ANI     2
00B5 CAA900             JZ      SCL2
00B8 3A2608             LDA     INTE    ;YES, CLEAR IT AND
00BB F680               ORI     80H     ;MAINTAIN INTERRUPT FLAG
00BD 320640             STA     4006H
00C0 3A2B08             LDA     HDFL    ;SEE IF TIME TO RAISE
00C3 3C                 INR     A
00C4 322B08             STA     HDFL
00C7 FE03               CPI     3
00C9 C2A900             JNZ     SCL2
00CC 97                 SUB     A       ;YES
00CD 320540             STA     4005H
00D0 322B08             STA     HDFL
00D3 060F       SCL1:   MVI     B,0FH   ;SET TO TEST ALL DRIVES
00D5 3A0018             LDA     1800H
00D8 1F                 RAR
00D9 DAE800             JC      ACTN
00DC CDBD02             CALL    DRAD    ;GET DRIVE ADDRESS
00DF CAD300             JZ      SCL1    ;JMP IF ALL DONE
00E2 CDE302             CALL    DRDY    ;TEST THIS DRIVE
00E5 C3D500             JMP     SCL1+2
                ; ACTION JUMP MODULE - PERFORMS COMMON OPERATIONS
                ; VERIFIES COMMAND STRING, THEN JUMPS TO PROPER ROUTINE
00E8 97         ACTN:   SUB     A       ;CLEAR INTERUPT FLAG
00E9 320640             STA     4006H
00EC 322608             STA     INTE
00EF 3A0014             LDA     1400H   ;GET COMMAND WORD
00F2 47                 MOV     B,A
00F3 E6F0               ANI     0F0H    ;GET TYPE
00F5 CA5401             JZ      ACT1    ;OF COMMAND STRING
00F8 C6F0               ADI     0F0H
00FA CA0F01             JZ      ACT2    ;POINTER SET
00FD C6F0               ADI     0F0H
00FF CA3401             JZ      ACT3    ;RESTORE DRIVE
0102 C6F0               ADI     0F0H
```

```
0104 CA4201            JZ    ACT4        ;SOFTWARE WRITE PROTECT
0107 C6F0              ADI   0F0H
0109 CA4701            JZ    ACT5        ;SOFTWARE WRITE ENABLE
010C C3A200            JMP   SCLP        ;NOP FUNCTION
010F CD2801    ACT2:   CALL  PADD        ;POINTER ADDRESS
0112 CD1C01            CALL  RBYT        ;LSB OF POINTER ADDRESS
0115 23                INX   H
0116 CD1C01            CALL  RBYT        ;MSB
0119 C3A200            JMP   SCLP
011C 3A0018    RBYT:   LDA   1800H       ;WAIT
011F 1F                RAR
0120 D21C01            JNC   RBYT
0123 3A0014            LDA   1400H       ;DATA
0126 77                MOV   M,A         ;SAVE
0127 C9                RET
0128 210008    PADD:   LXI   H,PBAS      ;BASE ADDRESS
012B 78                MOV   A,B
012C E60F              ANI   0FH
012E 07                RLC
012F 4F                MOV   C,A
0130 0600              MVI   B,0
0132 09                DAD   B
0133 C9                RET
0134 0E7F      ACT3:   MVI   C,7FH       ;RESTORE FLAG
0136 CDBD02            CALL  DRAD        ;GET DRIVE ADDRESS
0139 CAA200            JZ    SCLP
013C 7E                MOV   A,M
013D B1                ORA   C           ;SET NEW STATUS
013E 77                MOV   M,A
013F C33601            JMP   ACT3+2
0142 0E80      ACT4:   MVI   C,80H       ;PROTECT INDICATOR
0144 C33601            JMP   ACT3+2
0147 CDBD02    ACT5:   CALL  DRAD
014A CAA200            JZ    SCLP
014D 7E                MOV   A,M
014E E67F              ANI   7FH         ;CLEAR INDICATOR
0150 77                MOV   M,A
0151 C34701            JMP   ACT5
0154 CD2801    ACT1:   CALL  PADD
0157 4E                MOV   C,M         ;CONVERT TO TRUE ADDRESS
0158 23                INX   H
0159 66                MOV   H,M
015A 69                MOV   L,C         ;SECOND BYTE
015B 23                INX     H         ;SAVE STATUS BYTE ADDRESS...
015C 222908            SHLD    STPT
015F 2B                DCX     H
0160 CD9A03            CALL  FADD        ;TAKE CARE OF MSB
0163 0EC1              MVI   C,0C1H      ;SET FOR COMMAND STRING ERROR
0165 46                MOV   B,M         ;COMMAND
0166 23                INX   H
0167 3E00              MVI   A,0
0169 86                ADD   M
016A C28302            JNZ   AERX        ;STATUS BYTE NOT ZERO
016D 23                INX   H           ;TRACK MSB MUST BE ZERO
016E 86                ADD   M
016F C27F02            JNZ   AERX-4
0172 23                INX   H
0173 EB                XCHG
```

```
0174 CDBD02             CALL DRAD
0177 CA8202             JZ   AERX-1        ;NO DRIVE SELECTED
017A CDBD02             CALL DRAD
017D C28102             JNZ  AERX-2        ;MORE THAN ONE
0180 1A                 LDAX D             ;TRACK NUMBER
0181 13                 INX  D
0182 FE4D               CPI  77
0184 D27F02             JNC  AERX-4
0187 322008             STA  PTRK          ;SAVE
018A 322108             STA  LTRK
018D 78                 MOV  A,B           ;COMMAND
018E E6F0               ANI  0F0H
0190 CAA002             JZ   RDAL          ;READ ALL
0193 FEA1               CPI  0A1H
0195 D28002             JNC  AERX-3        ;ILLEGAL TOO LARGE
0198 FE60               CPI  60H
019A DAA201             JC   $+8
019D C6A0               ADI  0A0H
019F CA8002             JZ   AERX-3
01A2 322508             STA  FUNC          ;SAVE COMMAND
01A5 FE30               CPI  30H
01A7 CACA01             JZ   ACT6          ;JMP IF SECTOR NOT REQUIRED
01AA 1A                 LDAX D             ;GET IT
01AB 13                 INX  D
01AC B7                 ORA     A
01AD CA7E02             JZ   AERX-5
01B0 FE1B               CPI  27
01B2 D27E02             JNC  AERX-5
01B5 322208             STA  SECT          ;SAVE GOOD SECTOR VALUE
01B8 3A2508             LDA  FUNC          ;SEE IF NEED BUFFER LOC
01BB FE21               CPI  21H
01BD D2CA01             JNC  ACT6
01C0 1A         ACT7:   LDAX D             ;YES, GET IT
01C1 322308             STA  BUFA
01C4 13                 INX  D
01C5 1A                 LDAX D
01C6 13                 INX  D
01C7 322408             STA  BUFA+1
01CA 78         ACT6:   MOV  A,B           ;ALL PROCESSED, SEE IF IBM SPECIAL
01CB FE6F               CPI  6FH
01CD DADF01             JC   ACTQ
01D0 1A                 LDAX D             ;YES, GET LOGICAL TRACK
01D1 B7                 ORA     A
01D2 C27C02             JNZ     AERX-7
01D5 13                 INX  D
01D6 1A                 LDAX D
01D7 FE4D               CPI  77
01D9 D27C02             JNC  AERX-7
01DC 322108             STA  LTRK          ;SAVE IT
01DF 0EA1       ACTQ:   MVI  C,0A1H        ;SET DRIVE TEST ERROR
01E1 CDE302             CALL DRDY          ;SEE IF DRIVE READY
01E4 C28302             JNZ  AERX
01E7 78                 MOV  A,B           ;OKAY, SEE IF WRITE
01E8 E610               ANI  10H
01EA CAF901             JZ   ACT8
01ED 3A0440             LDA  4004H         ;YES, CHECK HARDWARE PROTECT
01F0 1F                 RAR
01F1 D28202             JNC  AERX-1
```

```
01F4 7E                 MOV   A,M
01F5 17                 RAL                 ;TEST SOFTWARE PROTECT
01F6 DA8102             JC    AERX-2        ;YES
01F9 97         ACT8:   SUB   A             ;SET PROCESSING FLAGS
01FA 322808             STA   RTRC          ;CLEAR RETRY COUNTER
01FD 322708             STA   INTF          ;SET INTERRUPT FLAG
0200 7E         ACTD:   MOV   A,M           ;NOW POSITION DRIVE
0201 E67F               ANI   7FH           ;GET PRESENT TRACK
0203 57                 MOV   D,A           ;SAVE STATUS OF PROTECT
0204 7E                 MOV   A,M
0205 E680               ANI   80H
0207 77                 MOV   M,A           ;SEEK NEW TRACK
0208 3A2008             LDA   PTRK
020B 86                 ADD   M
020C 77                 MOV   M,A
020D 3A2008             LDA   PTRK
0210 92                 SUB   D             ;GET DIFFERENCE
0211 1E00               MVI   E,0           ;SET FOR STEP IN
0213 57                 MOV   D,A
0214 CAAB02             JZ    TSTH          ;ALREADY ON TRACK
0217 F22302             JP    ACT9-4
021A 1E08               MVI   E,8           ;STEP OUT
021C 97                 SUB   A
021D 92                 SUB   D
021E 57                 MOV   D,A
021F 3A3108             LDA     SDRV        ;RAISE HEAD...
0222 320540             STA     4005H
0225 00                 NOP                 ;DELAY...
0226 00                 NOP
0227 15         ACT9:   DCR   D             ;TEST FOR TIME TO LOAD HEAD
0228 CC6A03             CZ    LDHD
022B 7B                 MOV   A,E           ;LOAD STEP REGISTER
022C 320640             STA   4006H
022F C604               ADI   4             ;NOW SET STEP BIT
0231 320640             STA   4006H
0234 E608               ANI   8             ;CLEAR STEP BIT
0236 C600               ADI   0
0238 320640             STA   4006H
023B FB         ACTP:   EI                  ;INTERRUPT IF DRIVE GOES NOT READY
023C CD8303             CALL  TMLD          ;WAIT 6 MILLISECONDS
023F CD8303             CALL  TMLD
0242 CD8303             CALL  TMLD
0245 15                 DCR   D             ;SEE IF MORE REQUIRED
0246 F22802             JP    ACT9+1
0249 1605               MVI   D,5           ;WAIT 10 MILLISECONDS FOR HEAD
024B CD8303             CALL  TMLD
024E 15                 DCR   D
024F C24B02             JNZ   $-4
                ;HEAD IS NOW LOADED, WE'RE ON RIGHT TRACK
                ;AND WE'RE READY TO TAKE ACTION
                ; RECALL THAT POINTER TO STATUS LOCATION IS SAVED
                ; IN STPT, FUNCTION IS IN 4 MSB OF FUNC
0252 F3         ACTB:   DI                  ;DISABLE INTERRUPT UNTIL REQUIRED
0253 3A2508             LDA   FUNC
0256 216A02             LXI   H,JMPT        ;BASE OF TABLE
0259 0F                 RRC
025A 0F                 RRC
025B 0F                 RRC
```

```
025C 0F                 RRC
025D E607               ANI   7
025F C26302     ACTA:   JNZ   $+4
0262 E9                 PCHL                ;JUMP TO ROUTINE
0263 23                 INX   H
0264 23                 INX   H
0265 23                 INX   H
0266 3D                 DCR   A
0267 C35F02             JMP   ACTA
                ;FOLLOWING IS JUMP TABLE FOR ACTIONS 0 TO 5
                ; NOTE THAT 7 TO 11 ARE SAME AS 0 TO 5 WITH DIFF LTRK
026A C3D703     JMPT:   JMP   RALL
026D C3D904             JMP   WRIT
0270 C36B05             JMP   READ
0273 C3EF05             JMP   FRMT
0276 C36B05             JMP   READ          ;JUST IGNORE TRANSFER AT END
0279 C32905             JMP   WDSC
                ;ERROR RETURN ROUTINE BASE ERROR IS IN C
027C 0C                 INR   C
027D 0C                 INR   C
027E 0C                 INR   C
027F 0C                 INR   C
0280 0C                 INR   C
0281 0C                 INR   C
0282 0C                 INR   C
0283 2A2908     AERX:   LHLD  STPT          ;GET STATUS BYTE ADDRESS
0286 CD9A03             CALL  FADD
0289 71                 MOV   M,C
028A F3                 DI                  ;INTERRUPTS OFF
028B 97                 SUB   A             ;CLEAR CONTROL REGISTERS
028C 320540             STA   4005H
028F 322B08             STA   HDFL
0292 3E10               MVI   A,10H
0294 320640             STA   4006H         ;SET INTERRUPT FLAG
0297 322608             STA   INTE
029A 310009             LXI   SP,STAK       ;RESET STACK POINTER
029D C3A200             JMP   SCLP
02A0 322508     RDAL:   STA   FUNC          ;SET FUNCTION
02A3 1A                 LDAX  D             ;GET DEAAY
02A4 13                 INX   D
02A5 322208             STA   SECT          ;SAVE IT
02A8 C3C001             JMP   ACT7          ;GO GET BUFFER LOC
02AB 3A2B08     TSTH:   LDA   HDFL          ;SEE IF HEAD LOAD REQUIRED
02AE B7                 ORA     A
02AF 3E01               MVI   A,1           ;ALREADY LOADED
02B1 322B08             STA   HDFL          ;RESET FLAG
02B4 C25202             JNZ   ACTB          ;GO PROCESS FUNCTION
02B7 CD6A03             CALL  LDHD
02BA C33B02             JMP   ACTP
                ; FORM DRIVE ADDRESS FOR DRIVE SELECTED IN 4 LSB OF B.
                ;   CLEAR BIT OF DRIVE SELECTED. RETURN NON-ZERO IF
                ;   THERE WAS A DRIVE AND ZERO IF NONE WAS SELECTED.
02BD 3E0F       DRAD:   MVI   A,0FH         ;SEE IF ANY
02BF A0                 ANA   B
02C0 C8                 RZ
02C1 3E01               MVI   A,1           ;0?
02C3 212C08             LXI   H,DRV0
02C6 A0                 ANA   B
```

```
02C7 C2DB02             JNZ   DRA1
02CA 3E02               MVI   A,2         ;1?
02CC 23                 INX   H
02CD A0                 ANA   B
02CE C2DB02             JNZ   DRA1
02D1 3E04               MVI   A,4         ;2?
02D3 23                 INX   H
02D4 A0                 ANA   B
02D5 C2DB02             JNZ   DRA1
02D8 3E08               MVI   A,8         ;MUST BE 3
02DA 23                 INX   H
02DB 323008     DRA1:   STA   TDRV        ;SAVE SELECT BIT
02DE 2F                 CMA               ;CLEAR THIS BIT
02DF A0                 ANA   B
02E0 47                 MOV   B,A
02E1 3C                 INR   A           ;SET FLAG
02E2 C9                 RET
                ; TEST DRIVE READY. RETURN NON-ZERO FLAG IF NOT READY.
                ; IF READY, PERFORM RESTORE IF FLAG SET (DRIVE TRACK = 7F).
02E3 3E01       DRDY:   MVI   A,1         ;SEE IF SELECTED
02E5 322708             STA   INTF        ;DRIVE IS READY
02E8 3A3008             LDA   TDRV        ;SELECT DRIVE AND
02EB 57                 MOV   D,A         ;SEE IF SAME AS LAST
02EC 3A3108             LDA   SDRV
02EF 92                 SUB   D
02F0 C2FA02             JNZ   DRD6
02F3 3A2B08             LDA   HDFL        ;SAME SEE IF HEAD DOWN
02F6 B7                 ORA     A
02F7 C20403             JNZ   DRD5        ;JUMP IF DOWN
02FA 97         DRD6:   SUB   A           ;CLEAR HEAD FLAG
02FB 322B08             STA   HDFL
02FE 3A3008             LDA   TDRV
0301 320540             STA   4005H
0304 FB         DRD5:   EI
0305 97                 SUB     A         ;IF DRIVE NOT READY, INTERRUPT
0306 F3                 DI                ;  OCCURS AND RETURNS A 1 IN A
0307 B7                 ORA     A
0308 C24003             JNZ   DRD1
030B 3A3008             LDA   TDRV        ;OKAY, SAVE DRIVE BIT
030E 323108             STA   SDRV
0311 7E                 MOV   A,M         ;CHECK FOR RESTORE FLAG
0312 E67F               ANI   7FH
0314 FE7F               CPI   7FH
0316 C23E03             JNZ   DRD2
0319 3A0440             LDA   4004H       ;YES, SEE IF OVER TRK 0
031C E604               ANI   4
031E C44B03             CNZ   STIN        ;IF SO, STEP IN
0321 3A0440             LDA   4004H       ;STILL THERE?
0324 E604               ANI   4
0326 C0                 RNZ               ;RETURN DRIVE NO GOOD
0327 164D               MVI   D,77        ;SET COUNT
0329 CD4F03     DRD3:   CALL  STOU        ;STEP OUT
032C 3A0440             LDA   4004H       ;THERE?
032F E604               ANI   4
0331 C23A03             JNZ   DRD4
0334 15                 DCR   D           ;NO, MAX TRIES?
0335 C22903             JNZ   DRD3
0338 14                 INR   D           ;SET NON-ZERO FLAG
```

```
0339 C9                 RET
033A 3E80       DRD4:   MVI   A,80H       ;THERE, SET TRACK 0
033C A6                 ANA   M
033D 77                 MOV   M,A
033E 97         DRD2:   SUB   A           ;SET ZERO FLAG
033F C9                 RET
0340 97         DRD1:   SUB   A           ;NOT READY, CLEAR HEAD FLAG
0341 322B08             STA   HDFL
0344 3E80               MVI   A,80H       ;SET RESTORE FLAG
0346 A6                 ANA   M
0347 C67F               ADI   7FH
0349 77                 MOV   M,A
034A C9                 RET
                ;STEP HEAD IN
034B 97         STIN:   SUB   A
034C C35103             JMP   STOU+2
                ;STEP HEAD OUT
034F 3E08       STOU:   MVI   A,8
0351 320640             STA   4006H
0354 C604               ADI   4           ;ADD STEP BIT
0356 320640             STA   4006H
0359 E608               ANI   8
035B C600               ADI   0
035D 320640             STA   4006H
0360 1606               MVI   D,6         ;WAIT 12 MILLISECONDS
0362 CD8303     STO1:   CALL  TMLD
0365 15                 DCR   D
0366 C26203             JNZ   STO1
0369 C9                 RET
                ; LOAD HEAD ROUTINE.  SET > 43 BIT IF REQUIRED
036A 7E         LDHD:   MOV   A,M         ;GET TRACK
036B E67F               ANI   7FH
036D FE2C               CPI   44
036F 3F                 CMC
0370 3E80               MVI   A,80H
0372 1F                 RAR
0373 0F                 RRC
0374 0F                 RRC
0375 4F                 MOV   C,A
0376 3A3108             LDA   SDRV        ;GET SELECT BIT
0379 81                 ADD   C
037A 320540             STA   4005H
037D 3E01               MVI   A,1         ;SET HEAD DOWN FLAG
037F 322B08             STA   HDFL
0382 C9                 RET
0383 CD8A03     TMLD:   CALL  MLDL        ;TWO MILLISECONDS IS
0386 CD8A03             CALL  MLDL        ;ONE PLUS ONE
0389 C9                 RET
038A 3E83       MLDL:   MVI   A,131
038C 3D                 DCR   A
038D C28C03             JNZ   $-1
0390 C9                 RET
                ;MOVE C BYTES FROM D TO H
0391 1A         DMOV:   LDAX  D
0392 77                 MOV   M,A
0393 13                 INX   D
0394 23                 INX   H
0395 0D                 DCR   C
```

```
0396 C29103             JNZ   DMOV
0399 C9                 RET
039A 7C         FADD:   MOV   A,H          ;SET MEMORY BIT FOR TRANSFER
039B E680               ANI   80H
039D 0F                 RRC
039E 0F                 RRC
039F 320640             STA   4006H
03A2 7C                 MOV   A,H          ;SET BIT 15 FOR INTERNAL
03A3 F680               ORI   80H
03A5 67                 MOV   H,A
03A6 C9                 RET
                ;
0048 =          CRCU    EQU     48H
0029 =          CRCL    EQU     29H
                ;
                ; COMPUTE CRC FROM BUFFER POINTED TO BY PAIR D
                ; BUFFER LENGTH IS IN C
                ;
03A7 21FFFF     CRCC:   LXI   H,0FFFFH     ;PRESET CRC VALUE
03AA 1A                 LDAX  D            ;GET A BYTE
03AB CDB403             CALL  CRC1         ;DO ONE BYTE
03AE 13                 INX   D
03AF 0D                 DCR   C
03B0 C2AA03             JNZ   CRCC+3
03B3 C9                 RET
03B4 C5         CRC1:   PUSH  B            ;COMPUTE FOR ONE BYTE
03B5 D5                 PUSH  D
03B6 AC                 XRA   H
03B7 47                 MOV   B,A
03B8 07                 RLC
03B9 07                 RLC
03BA 07                 RLC
03BB 07                 RLC
03BC A8                 XRA   B
03BD 4F                 MOV   C,A
03BE E6F0               ANI   0F0H
03C0 57                 MOV   D,A
03C1 81                 ADD   C
03C2 5F                 MOV   E,A
03C3 7A                 MOV   A,D
03C4 CE00               ACI   0
03C6 AD                 XRA   L
03C7 67                 MOV   H,A
03C8 78                 MOV   A,B
03C9 E6F0               ANI   0F0H
03CB 47                 MOV   B,A
03CC A8                 XRA   E
03CD 6F                 MOV   L,A
03CE 78                 MOV   A,B
03CF 0F                 RRC
03D0 0F                 RRC
03D1 0F                 RRC
03D2 AC                 XRA   H
03D3 67                 MOV   H,A
03D4 D1                 POP   D
03D5 C1                 POP   B
03D6 C9                 RET
                ;READ ALL LOOP...INTERLEAVE CLOCK AND DATA (64 BYTES WORTH)
```

```
03D7 0E40       RALL:   MVI   C,64        ;BYTE COUNTER
03D9 3E80               MVI   A,80H       ;INHIBIT INDEX INTERRUPT
03DB 320640             STA   4006H
03DE 31B708             LXI   SP,DATB+1   ;SET DATA AREA
03E1 FB                 EI
03E2 3A0440     RAL1:   LDA   4004H       ;WAIT FOR INDEX
03E5 E602               ANI   2
03E7 CAE203             JZ    RAL1
03EA 3A2208             LDA   SECT
03ED FE00               CPI   0
03EF CAFA03             JZ    RAL2
03F2 57                 MOV   D,A
03F3 CD8A03             CALL  MLDL
03F6 15                 DCR   D
03F7 C2F303             JNZ   $-4
03FA 3E01       RAL2:   MVI   A,1         ;SYNC PLO
03FC 320640             STA   4006H
03FF 97                 SUB   A
0400 C600               ADI   0           ;DELAY 12 MICROSECONDS
0402 C600               ADI   0
0404 320640             STA   4006H
0407 2A0240     RAL4:   LHLD  4002H       ;GET 64 BYTES WORTH
040A E5                 PUSH  H
040B 0D                 DCR   C
040C C20704             JNZ   RAL4
040F 2A2308     RAL7:   LHLD  BUFA        ;MOVE TO MAIN MEMORY
0412 CD9A03             CALL  FADD
0415 11B608             LXI   D,DATB
0418 0E80               MVI   C,128
041A 1A         RAL5:   LDAX  D
041B 1B                 DCX   D
041C 77                 MOV   M,A
041D 23                 INX   H
041E 0D                 DCR   C
041F C21A04             JNZ   RAL5
0422 2A2908     RAL6:   LHLD  STPT        ;SUCCESSFUL RETURN
0425 CD9A03             CALL  FADD
0428 F3                 DI
0429 34                 INR   M
042A 3E10               MVI   A,10H       ;SET INTERRUPT FLAG
042C 320640             STA   4006H
042F 322608             STA   INTE        ;AND SAVE THE SET VALUE
0432 310009             LXI   SP,STAK     ;RESET STACK POINTER
0435 C3A200             JMP   SCLP        ;WAIT FOR MORE
                ;ROUTINE TO SYNC ON START OF SECTOR
                ;EXITS AFTER TEN BYTES OF ZEROES FOLLOWING HEADER
0438 CD4E05     SYNC:   CALL  HDRC        ;COMPUTE CRC FOR HEADER
043B E5                 PUSH  H           ;SAVE FOR LATER
043C 97         SYN2:   SUB   A           ;CLEAR INDEX COUNTER
043D 322608             STA   INTE
0440 110240             LXI   D,4002H     ;REGISTER ADDRESS
0443 3A2108             LDA   LTRK        ;SET FOR FAST CHECKING
0446 4F                 MOV   C,A
0447 3A2208             LDA   SECT
044A 47                 MOV   B,A
044B 31FC08             LXI   SP,STAK-4   ;WHERE CRC IS STORED
044E 3A0440             LDA   4004H       ;TEST FOR INDEX
0451 E602               ANI   2
```

```
0453 CA6F04             JZ    SYN1
0456 3E80               MVI   A,80H       ;CLEAR IT
0458 320640             STA   4006H
045B 3A2608             LDA   INTE        ;YES, SEE IF SECOND
045E 3C                 INR   A
045F 322608             STA   INTE
0462 FE03               CPI   3
0464 C26F04             JNZ   SYN1
0467 0E93               MVI   C,93H       ;SECOND SET ERROR
0469 CDE205     SYN4:   CALL  RTRY        ;SEE IF RETRY COUNT EXPIRED
046C C33C04             JMP   SYN2        ;RETURN SAYS TRY AGAIN
046F 3E01       SYN1:   MVI   A,1         ;SYNC PLO
0471 320640             STA   4006H
0474 97                 SUB   A
0475 E3                 XTHL
0476 E3                 XTHL
0477 C600               ADI   0
0479 320640             STA   4006H
047C FB                 EI
047D 3EC7               MVI   A,0C7H      ;WAIT FOR CHARACTER
047F 2A0040             LHLD  4000H
0482 BC                 CMP   H
0483 C24004             JNZ   SYN2+4      ;CLOCK PATTERN CHECK
0486 2C                 INR   L           ;DATA SHOULD BE FC
0487 1A                 LDAX  D           ;GET TRACK
0488 91                 SUB   C
0489 C2B404             JNZ   SYN3        ;NOT SAME - WRONG TRACK?
048C 2C                 INR   L           ;COMPLETE DATA BYTE CHECK
048D EB                 XCHG
048E 4E                 MOV   C,M         ;GET ZERO BYTE
048F C24004             JNZ   SYN2+4      ;JMP IF DATA BYTE NOT CORRECT
0492 D1                 POP   D           ;GET CRC BYTES
0493 7E                 MOV   A,M         ;GET SECTOR
0494 90                 SUB   B           ;CORRECT?
0495 C24004             JNZ   SYN2+4
0498 79                 MOV   A,C         ;YES
0499 B6                 ORA   M           ;LAST ZERO BYTE
049A 0E95               MVI   C,95H
049C C26904             JNZ   SYN4        ;JUMP ON FORMAT ERROR
049F 7E                 MOV   A,M         ;CRC BYTE 1
04A0 92                 SUB   D           ;CHECK IT
04A1 C2A604             JNZ   $+5
04A4 7B                 MOV   A,E
04A5 96                 SUB   M           ;CHECK CRC BYTE 2
04A6 0E94               MVI   C,94H
04A8 C26904             JNZ   SYN4        ;JUMP ON ERROR
04AB 7E                 MOV   A,M         ;OKAY, WAIT TEN BYTES
04AC 0E09               MVI   C,9
04AE 7E                 MOV   A,M
04AF 0D                 DCR   C
04B0 C2AE04             JNZ   $-2
04B3 C9                 RET               ;RETURN OKAY
04B4 2C         SYN3:   INR   L           ;SEE IF DATA BYTE CORRECT
04B5 C24004             JNZ   SYN2+4
04B8 F3                 DI                ;YES, THERE IS TRACK ADDRESS ERROR
04B9 3A3108             LDA   SDRV        ;SET DRIVE FOR RESTORE
04BC 47                 MOV   B,A
04BD 310009             LXI   SP,STAK     ;CORRECT SP
```

```
04C0 CDBD02             CALL DRAD
04C3 3E80               MVI  A,80H
04C5 A6                 ANA  M
04C6 C67F               ADI  7FH
04C8 77                 MOV  M,A
04C9 0E92               MVI  C,92H      ;SEE IF RETRY DONE
04CB CDE205             CALL RTRY
04CE CDE302             CALL DRDY       ;OKAY, POSITION DRIVE AGAIN
04D1 CA0002             JZ   ACTD       ;OVER 0 THEN GO AGAIN
04D4 0E91               MVI  C,91H      ;DRIVE INOPERABLE
04D6 C38302             JMP  AERX
                ;ROUTINE TO WRITE A DATA BLOCK
04D9 2A2308     WRIT:   LHLD BUFA       ;FIRST GET DATA
04DC CD9A03             CALL FADD
04DF 113208             LXI  D,DATB-132
04E2 D5                 PUSH D
04E3 EB                 XCHG
04E4 36FB               MVI  M,0FBH     ;DATA HEADER FOR CRC
04E6 23                 INX  H
04E7 0E80               MVI  C,128
04E9 CD9103             CALL DMOV
04EC D1                 POP  D          ;GET DATA ADDRESS AGAIN
04ED 0E81               MVI  C,129
04EF CDA703             CALL CRCC
04F2 7C                 MOV  A,H        ;SAVE IT
04F3 12                 STAX D
04F4 13                 INX  D
04F5 7D                 MOV  A,L
04F6 12                 STAX D
04F7 13                 INX  D
04F8 97                 SUB  A          ;TRAILING ZERO
04F9 12                 STAX D
04FA CD3804             CALL SYNC       ;FIND PROPER SECTOR
04FD 210740             LXI  H,4007H    ;SET WRITE ADDRESS
0500 014205             LXI  B,542H     ;SET COUNTERS
0503 313308             LXI  SP,DATB-131
0506 D1                 POP  D          ;GET FIRST DATA BYTES
0507 3E02               MVI  A,2        ;SET WRITE ENABLE
0509 320640             STA  4006H
050C 97                 SUB  A          ;WRITE ZERO BYTES
050D 05                 DCR  B
050E 77                 MOV  M,A
050F C20D05             JNZ  $-2
0512 3EFB               MVI  A,0FBH     ;WRITE DATA INDEX MARK
0514 321F40             STA  401FH
0517 C31C05             JMP  $+5        ;START DATA LOOP
051A 72         WRT2:   MOV  M,D
051B D1                 POP  D          ;GET NEXT TWO BYTES OF DATA
051C 0D                 DCR  C          ;SEE IF DONE
051D 73                 MOV  M,E        ;WRITE DATA BYTE
051E C21A05             JNZ  WRT2
0521 73                 MOV  M,E        ;WAIT FOR ZERO BYTE
0522 97                 SUB  A          ;CLEAR WRITE ENABLE
0523 320640             STA  4006H
0526 C32204             JMP  RAL6       ;SUCCESSFUL RETURN
                ;ROUTINE TO WRITE DELETED DATA ADDRESS MARK
0529 CD3804     WDSC:   CALL SYNC       ;FIND SECTOR
052C 210740             LXI  H,4007H    ;DATA WRITE REGISTER
```

```
052F 010105             LXI  B,501H     ;SET COUNTERS
0532 3C                 INR  A          ;EQUALIZE TIME WITH WRITE
0533 3C                 INR  A
0534 3C                 INR  A
0535 3C                 INR  A
0536 3E02               MVI  A,2        ;SET WRITE ENABLE
0538 320640             STA  4006H
053B 97                 SUB  A
053C 05                 DCR  B          ;WRITE ZERO BYTES
053D 77                 MOV  M,A
053E C23C05-            JNZ  $-2
0541 3EF8               MVI  A,0F8H     ;WRITE DELETED DATA HEADER
0543 321F40             STA  401FH
0546 97                 SUB  A          ;TRAILING HEADER
0547 77                 MOV  M,A
0548 320640             STA  4006H      ;CLEAR WRITE ENABLE
054B C32204             JMP  RAL6       ;SUCCESSFUL RETURN
054E 21FFFF     HDRC:   LXI  H,0FFFFH   ;COMPUTE HEADER CRC
0551 3EFE               MVI  A,0FEH     ;ADDRESS INDEX MARK
0553 CDB403             CALL CRC1
0556 3A2108             LDA  LTRK       ;TRACK ADDRESS
0559 CDB403             CALL CRC1
055C 97                 SUB  A          ;ZERO BYTE
055D CDB403             CALL CRC1
0560 3A2208             LDA  SECT       ;SECTOR NUMBER
0563 CDB403             CALL CRC1
0566 97                 SUB  A          ;ZERO BYTE
0567 CDB403             CALL CRC1       ;IT IS ALL COMPUTED IN H,L NOW
056A C9                 RET
                ;ROUTINE TO READ A SECTOR OF DATA
056B CD3804     READ:   CALL SYNC       ;FIND SECTOR
056E 110240             LXI  D,4002H    ;DATA READ ADDRESS
0571 014106             LXI  B,641H     ;SET COUNTERS
0574 31B708             LXI  SP,DATB+1  ;SET DATA BUFFER READ POINTER
0577 05                 DCR  B          ;DELAY PAST HEAD TURN ON AREA
0578 C27705             JNZ  $-1
057B 3E01               MVI  A,1        ;SYNC PLO
057D 320640             STA  4006H
0580 97                 SUB  A
0581 E3                 XTHL
0582 E3                 XTHL
0583 E3                 XTHL
0584 E3                 XTHL
0585 320640             STA  4006H
0588 3EC7               MVI  A,0C7H     ;SET UP FOR TESTING DATA
058A 06FB               MVI  B,0FBH     ;ADDRESS MARK
058C 2A0040             LHLD 4000H      ;READ IT FROM DISK
058F 94                 SUB  H          ;CHECK CLOCK PATTERN
0590 C2D905             JNZ  RED1
0593 EB                 XCHG
0594 56                 MOV  D,M        ;GET FIRST DATA BYTE
0595 7B                 MOV  A,E        ;TEST DATA FROM INDEX MARK
0596 90                 SUB  B
0597 C2CF05             JNZ  RED4       ;JMP TO SEE IF DELETED DATA
059A 5E         RED2:   MOV  E,M        ;ALL OKAY, GET ANOTHER DATA BYTE
059B D5                 PUSH D          ;STORE TWO OF THEM
059C 0D                 DCR  C
059D 56                 MOV  D,M        ;GET NEXT BYTE
```

```
059E C29A05             JNZ   RED2         ;LOOP UNTIL DONE
05A1 5E                 MOV   E,M          ;THIS IS SECOND OF CRC BYTES
05A2 D5                 PUSH  D            ;SAVE THEM
05A3 F3                 DI                 ;ALL DONE
05A4 310009             LXI   SP,STAK
05A7 21FFFF             LXI   H,0FFFFH     ;NOW CHECK CRC
05AA 11B608             LXI   D,DATB
05AD 0E82               MVI   C,130
05AF 3EFB               MVI   A,0FBH       ;FIRST DO HEADER DATA
05B1 CDB403             CALL  CRC1
05B4 1A         RED3:   LDAX  D            ;GET DATA BYTE
05B5 CDB403             CALL  CRC1
05B8 1B                 DCX   D
05B9 0D                 DCR   C            ;SEE IF DONE
05BA C2B405             JNZ   RED3
05BD 7C                 MOV   A,H          ;SEE IF CRC CORRECT
05BE B5                 ORA   L
05BF C2D905             JNZ   RED1
05C2 3A2508             LDA   FUNC         ;OKAY, SEE IF CHECK READ
05C5 E6F0               ANI   0F0H
05C7 FE20               CPI   20H
05C9 CA0F04             JZ    RAL7         ;GO MORE DATA IFF READ
05CC C32204             JMP   RAL6         ;SUCCESSFUL RETURN IF CHECK READ
05CF C603       RED4:   ADI   3            ;TEST FOR DELETED DATA
05D1 C2D905             JNZ   RED1
05D4 0E97               MVI   C,97H        ;YES, SET ERROR
05D6 C38302             JMP   AERX         ;  AND RETURN
05D9 0E96       RED1:   MVI   C,96H        ;CRC ERROR
05DB F3                 DI
05DC CDE205             CALL  RTRY         ;SEE IF TRY AGAIN
05DF C36B05             JMP   READ         ;YES
                ;TEST RETRY COUNTER. RETURN IF TIME TO TRY AGAIN
05E2 3A2808     RTRY:   LDA   RTRC         ;INCREMENT RETRY COUNTER
05E5 3C                 INR   A
05E6 322808             STA   RTRC
05E9 FE0B               CPI   11           ;SEE IF ALL DONE
05EB C0                 RNZ
05EC C38302             JMP   AERX         ;TRIED MAX TIMES, SO QUIT
                ;ROUTINE TO FORMAT A TRACK OF A DISKETTE
05EF 3E1A       FRMT:   MVI   A,26         ;COMPUTE AND SAVE HEADER
05F1 322208             STA   SECT         ;CRC VALUES FOR ALL 26 SECTORS
05F4 11B608             LXI   D,DATB
05F7 CD4E05     FRM1:   CALL  HDRC
05FA 7D                 MOV   A,L
05FB 12                 STAX  D
05FC 1B                 DCX   D
05FD 7C                 MOV   A,H
05FE 12                 STAX  D
05FF 1B                 DCX   D            ;CRC SAVED
0600 3A2208             LDA   SECT         ;SET NEXT SECTOR
0603 3D                 DCR   A
0604 322208             STA   SECT
0607 C2F705             JNZ   FRM1         ;LOOP UNTIL 26 DONE
060A 13                 INX   D            ;SET D TO CRC OF FIRST SECTOR
060B 210740             LXI   H,4007H      ;WRITE REGISTER
060E 012C01             LXI   B,12CH       ;SET COUNTERS
0611 3E80               MVI   A,80H
0613 320640             STA   4006H        ;WAIT FOR INDEX
```

```
0616 FB                 EI
0617 3A0440             LDA   4004H
061A E602               ANI   2
061C CA1706             JZ    $-5
061F 3E82               MVI   A,82H       ;SET WRITE ENABLE
0621 320640             STA   4006H
0624 97                 SUB   A           ;SET ZERO BYTES
0625 77                 MOV   M,A
0626 0D                 DCR   C           ;WRITE GAP 4
0627 C22506             JNZ   $-2
062A 77                 MOV   M,A
062B 3EFC               MVI   A,0FCH      ;WRITE INDEX ADDRESS MARK
062D 321740             STA   4017H
0630 97         FRM2:   SUB   A           ;DO A SECTOR'S WORTH
0631 0E1E               MVI   C,30        ;FOR GAP 1
0633 77                 MOV   M,A
0634 0D                 DCR   C
0635 C23306             JNZ   $-2
0638 77                 MOV   M,A         ;LAST BYTE
0639 3EFE               MVI   A,0FEH      ;ID ADDRESS MARK
063B 321F40             STA   401FH
063E 3A2108             LDA   LTRK        ;TRACK ADDRESS
0641 77                 MOV   M,A
0642 97                 SUB   A           ;ZERO BYTE
0643 77                 MOV   M,A
0644 0E10               MVI   C,16        ;SET COUNT FOR GAP 2
0646 70                 MOV   M,B         ;SECTOR NUMBER
0647 77                 MOV   M,A         ;ZERO BYTE
0648 1A                 LDAX  D           ;CRC BYTE 1
0649 13                 INX   D
064A 77                 MOV   M,A
064B 1A                 LDAX  D           ;CRC BYTE 2
064C 13                 INX   D
064D 77                 MOV   M,A
064E 97                 SUB   A           ;ZERO BYTES FOR GAP 2
064F 0D                 DCR   C
0650 C24D06             JNZ   $-3
0653 77                 MOV   M,A         ;LAST BYTE
0654 3EFB               MVI   A,0FBH      ;DATA ADDRESS MARK
0656 321F40             STA   401FH
0659 97                 SUB   A           ;DATA BYTES FOR SECTOR ARE ALL ZERO
065A 0E7F               MVI   C,127       ;NUMBER BYTES LESS ONE
065C 77                 MOV   M,A         ;WRITE ONE
065D 0D                 DCR   C
065E C25C06             JNZ   $-2
0661 77                 MOV   M,A         ;LAST BYTE
0662 3E48               MVI   A,CRCU
0664 77                 MOV   M,A
0665 3E29               MVI   A,CRCL
0667 77                 MOV   M,A
0668 04                 INR   B           ;ADVANCE SECTOR NUMBER
0669 3E1B               MVI   A,27
066B 90                 SUB   B
066C 71                 MOV   M,C         ;WRITE ZERO BYTE
066D C23006             JNZ   FRM2        ;LOOP TILL DONE
0670 3A0440     FRM4:   LDA   4004H       ;WRITE ZEROES TO INDEX
0673 71                 MOV   M,C
0674 E602               ANI   2
```

```
0676 C27D06             JNZ   FRM3
0679 71                 MOV   M,C
067A C37006             JMP   FRM4
067D 97         FRM3:   SUB   A           ;CLEAR WRITE ENABLE
067E 320640             STA   4006H
0681 C32204             JMP   RAL6
0684                    END
```

FLOPPY DISK SYSTEM

FLOPPY POWER SUPPLY

FUNCTIONAL DESCRIPTION----------

The Universal Floppy Power Supply, (FPS-U), is designed to support the CalComp Model 140(60 HZ) or 140B(50 HZ) Floppy Disk Drives. It provides for all power and signal connections to the Drive and allows up to four (Floppy Drive and FPS-U) modules to be used in a Daisy Chain configuration. The FPS-U Assembly supports up to seven input voltages as listed in Table 1.

POWER SUPPLIES: The Power Supply section provides independent, fully regulated +5 and +24 volts at the current levels required to support the Model 140/140B Drive. AC Supply Lines are fused and the DC Regulators provide ample protection for the Drive circuits.

Power ON/OFF switching is User selectable to operate in the switched or unswitched mode, allowing multiple drives to be switched on or off from a single source.

SIGNAL BUSSING: The signal bussing arrangement provides for up to four Drives and one PLO to be used in a Daisy Chained configuration. Provision is made for all required Bus Termination resistors. Cabling is done with the Scotchflex Flat Cable and Connector System; and the FPS-U is easily removed from the Drive for servicing with no unsoldering of connections.

DRIVE NUMBER SELECTION: User options allow Jumper selection of the Daisy Chain Drive Number to be used with a particular FPS-U.

PACKAGING: The FPS-U Chassis is designed to mount directly to the rear of the Model 140/140B Drive, with no additional modifications. The dimensions of the FPS-U allow multiple FPS-U-Drive Modules to be stacked, either vertically or horizontally, with no interference problems. A cooling duct and chassis cutouts allow for unrestricted air flow and cooling of the drive and FPS-U.

TABLE 1

IMSAI FPS-U MODEL	INPUT VOLTAGE AC	FREQ.	CALCOMP DRIVE MODEL #
FPS-U 100/60	100 VAC	60 HZ	140-005
FPS-U 208/60	208 VAC	60 HZ	140-006
FPS-U 230/60	230 VAC	60 HZ	140-002
FPS-U 100/50	100 VAC	50 HZ	140B-004
FPS-U 208/50	208 VAC	50 HZ	140B-005
FPS-U 220/50	220 VAC	50 HZ	140B-005
FPS-U 240/50	240 VAC	50 HZ	140B-006

NOTE: Differences between models at FPS-U are in the wiring of the transformer (see the Assembly Instructions).

NOTE: All AC input voltages are ±10%; 50 and 60 HZ are ±.5% tolerance.

THEORY OF OPERATION----------

The FPS-U consists of two functionally distinct sections: 1) Power Supply Circuits; and 2) Signal Bus.

POWER SUPPLY: The Power Supply section consists of two independent, regulated +5 VDC and +24 VDC supplies.

The diode bridge composed of CR1-CR4, driven by the secondary of Transformer T2, provides an unregulated 12 volts DC. Capacitor C2 acts to filter the raw 12VDC output; and Q1 and A3 are used in a Current Sharing configuration to provide a regulated +5 VDC at 1.0 Amps.

Similarly, the diode bridge composed of CR5-CR8, driven by the secondary of Transformer T1, provides an unregulated 28 VDC. Capacitor C1 acts to filter the raw 28 VDC output; and Q2 and A2 are used in a Current Sharing configuration to provide the regulated +24 VDC at 1.5 Amps.

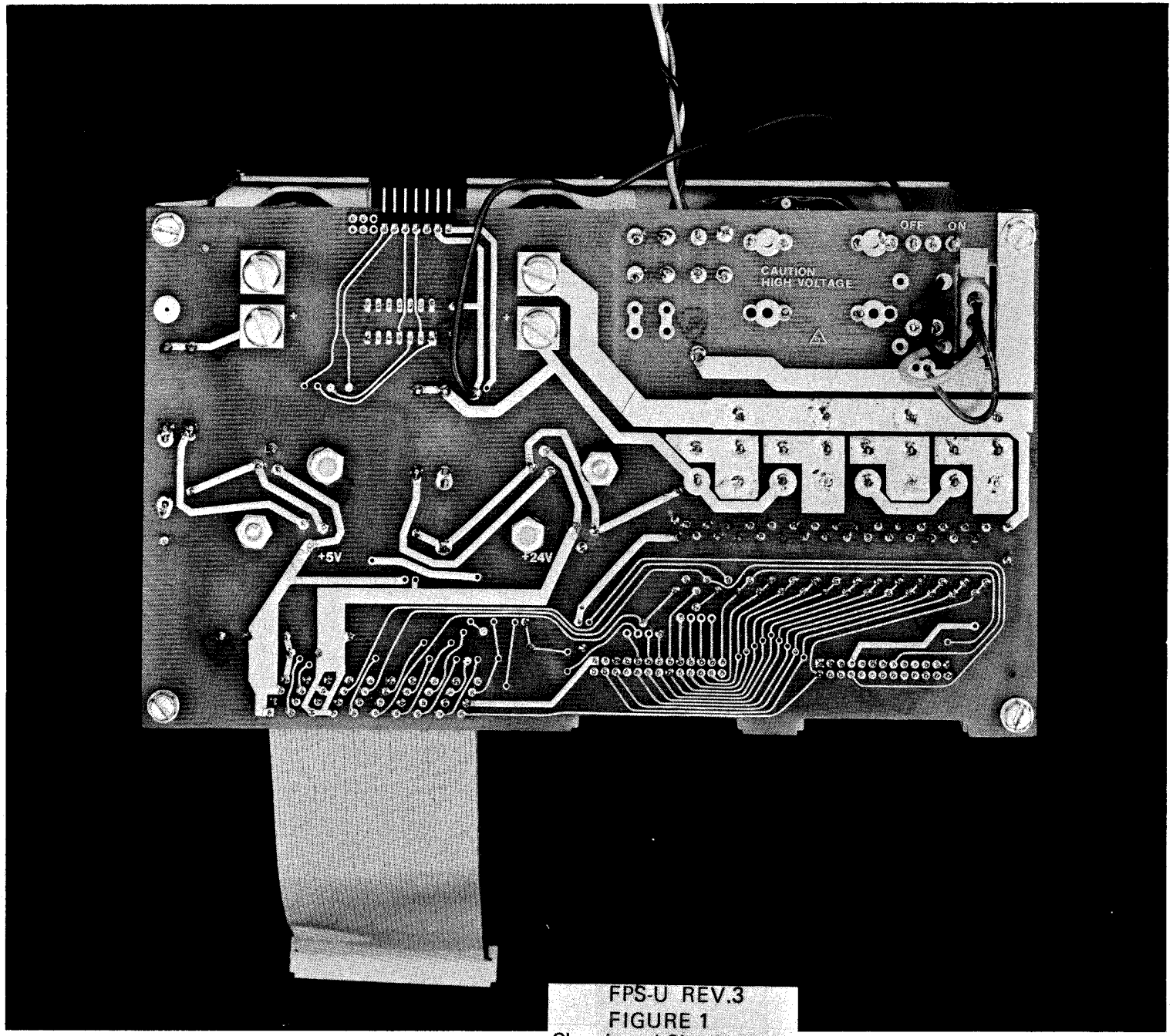
SIGNAL BUS: The 26 pin bus connectors (J2 and J3), are connected in parallel to support a Daisy Chain of up to four Drives. A single 40 pin Flat Cable connects the bus signals, from J2 and J3, to the Floppy Disk Drive.

Jumper Areas A and B allow the READY and SELECT lines from a Drive to be jumpered to one of four pairs of READY and SELECT lines on the 26 pin signal bus.

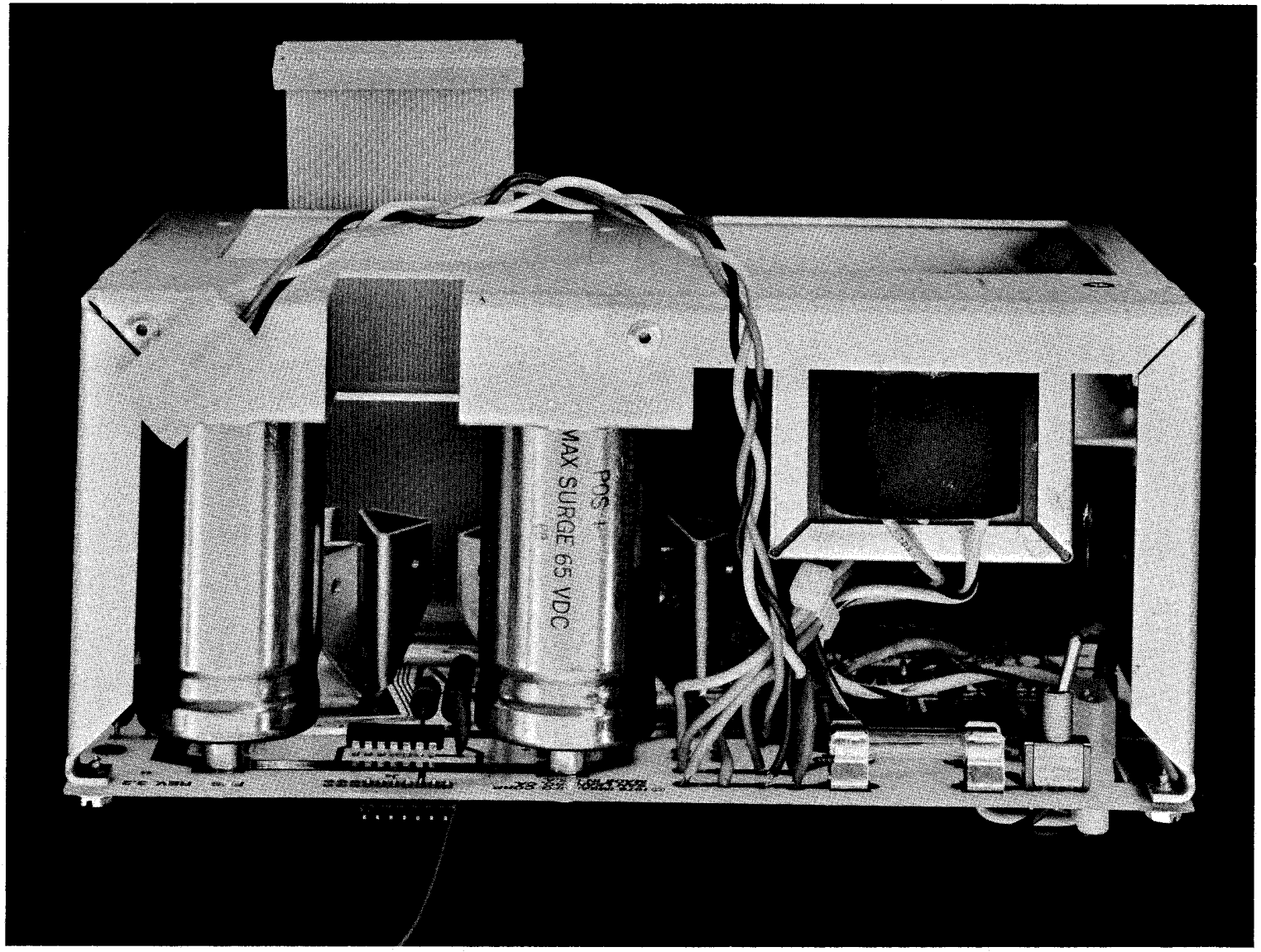
NOTE: The READY and SELECT lines are the only signal lines which are unique to any one Drive. Therefore the configuration of Jumper Areas A and B determines the number of the Drive in the Daisy Chain.

TERMINATION RESISTORS: All signal lines on the 26 pin bus are terminated to establish the correct quiescent voltage levels and to minimize noise. Each FPS-U contains selected termination resistors according to its position in the Daisy Chain (TABLE 2- ASSEMBLY INSTRUCTIONS).

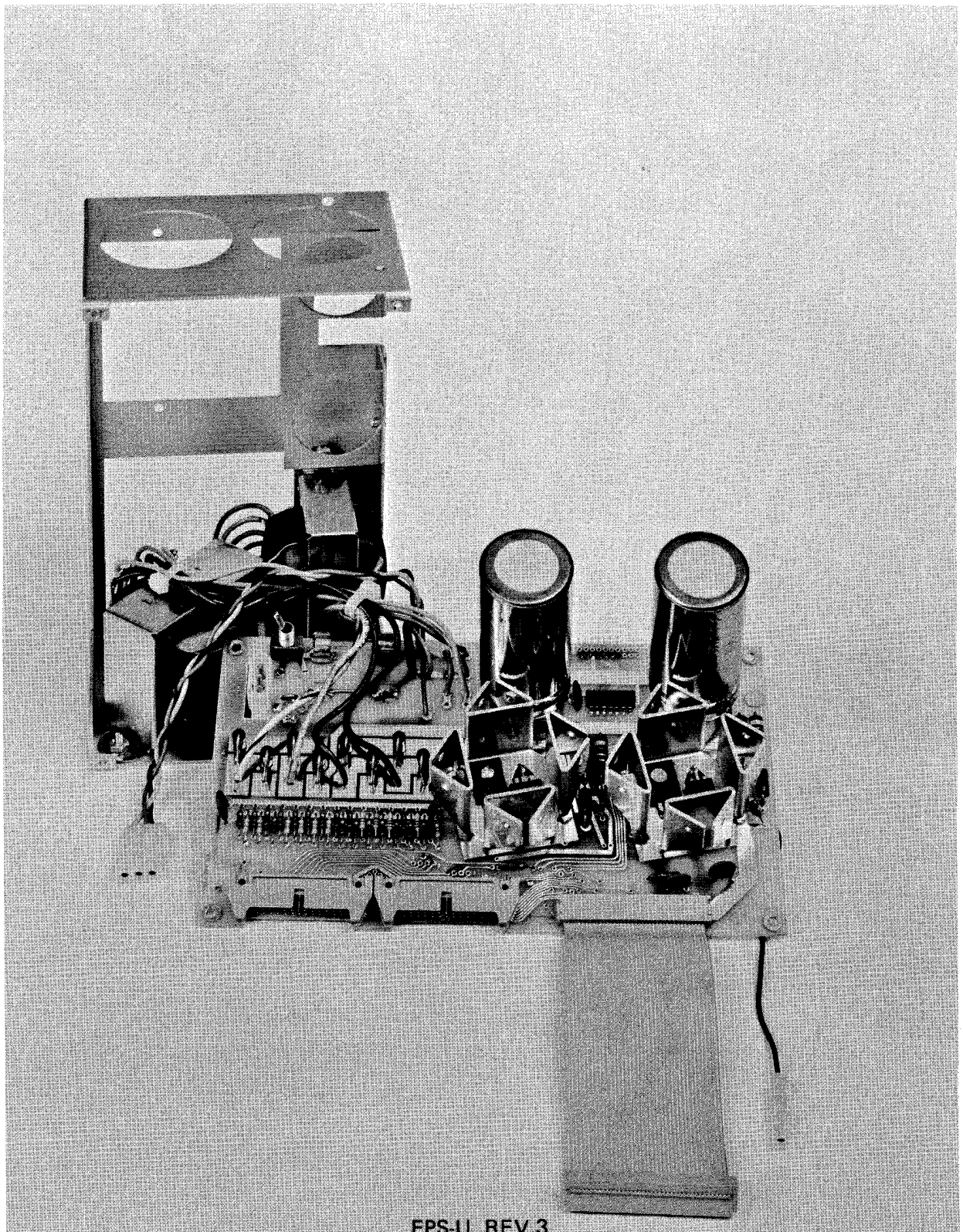
PLO SIGNALS: J4 of the FPS-U used with Drive 0 will connect to the 26-pin signal bus. Note that only one PLO Board is needed for up to four Drives. For all Drives except Drive 0, a Jumper must be installed at FPS-U board location J6. This allows the PLO /READ CLOCK line to be correctly placed on the 26-pin signal bus.



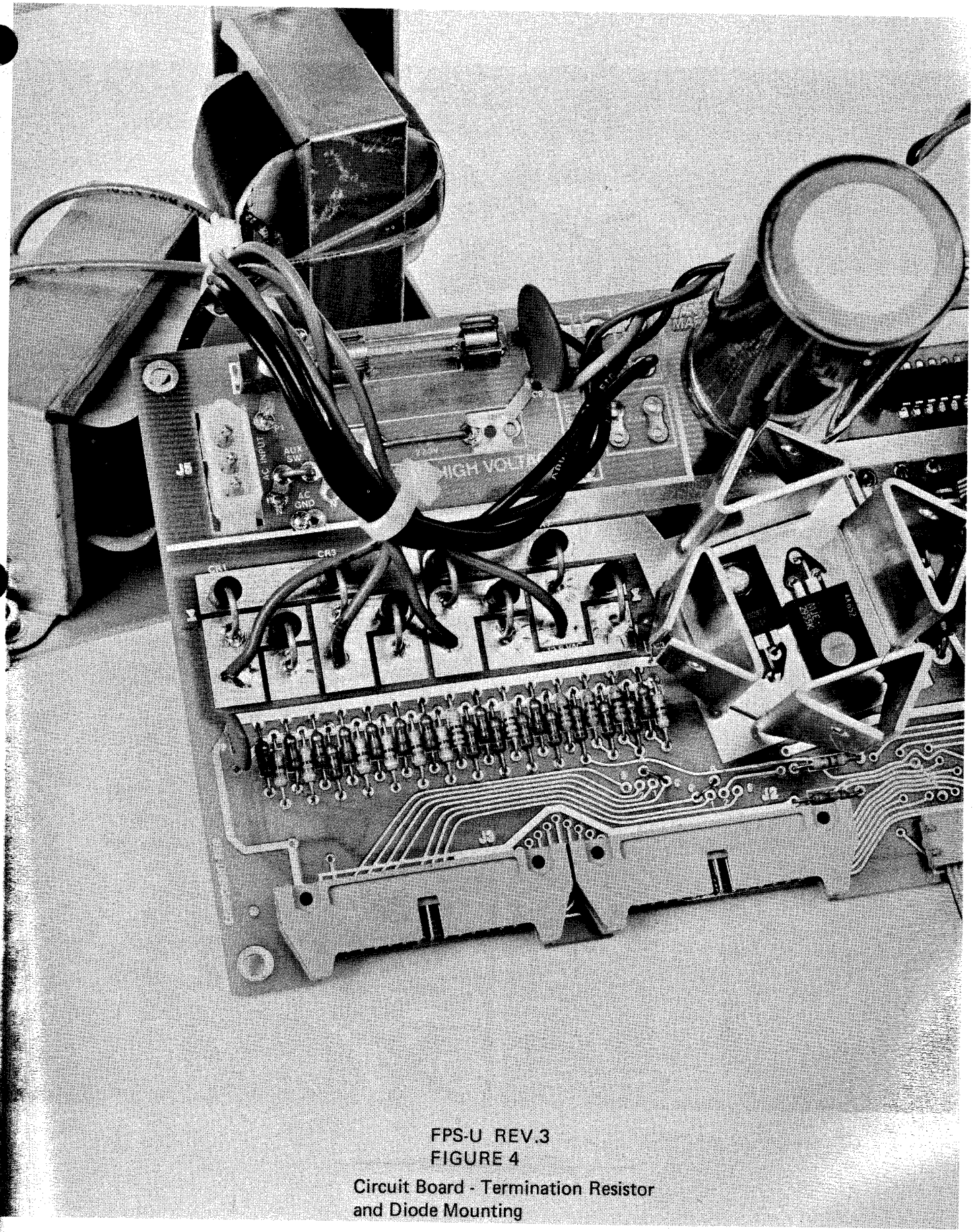
FPS-U REV.3
FIGURE 1
Chassis and Circuit Board Assembly- Bottom View



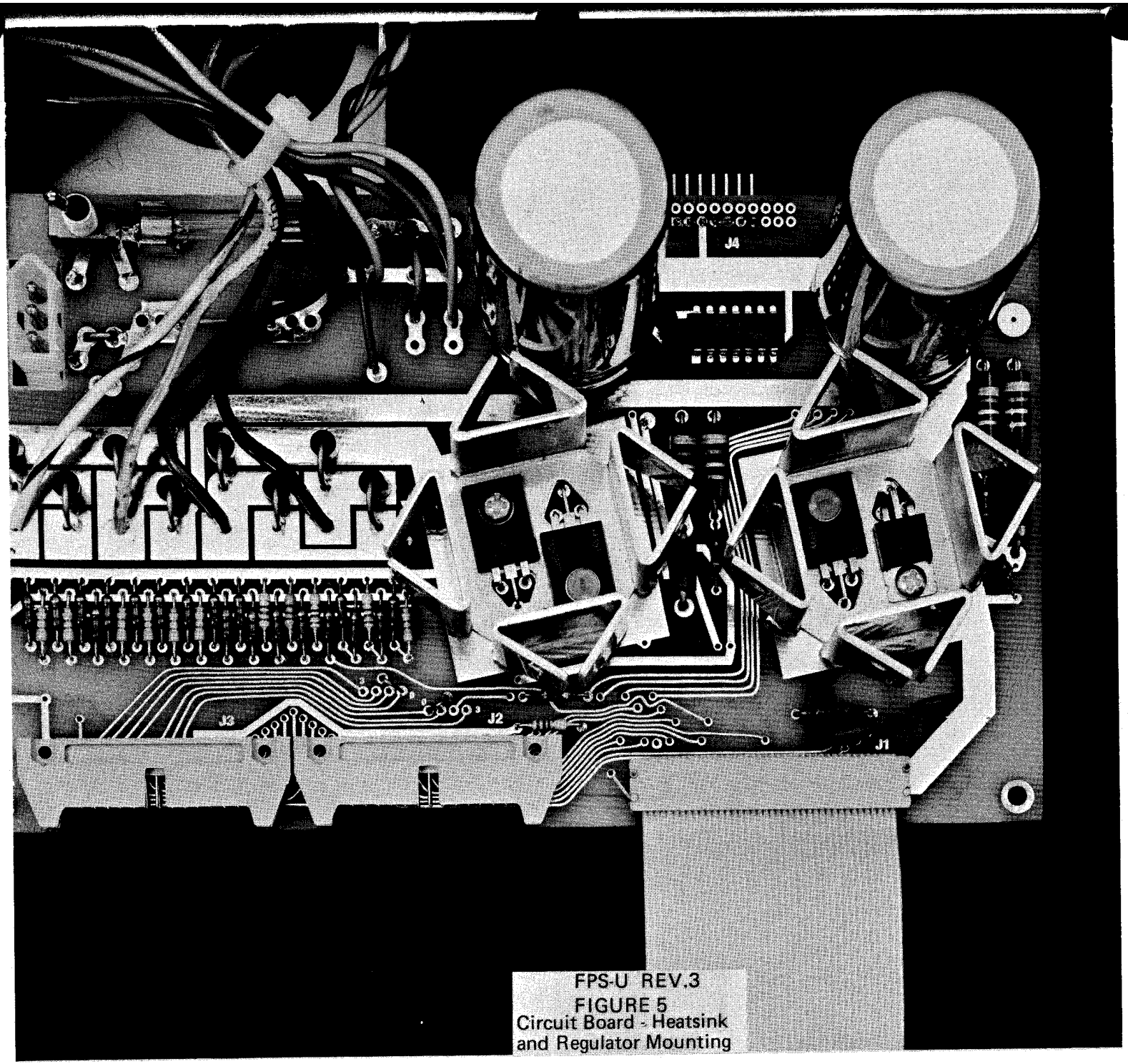
FPS-U REV.3
FIGURE 2
Chassis and Circuit Board
Assembly - Side View



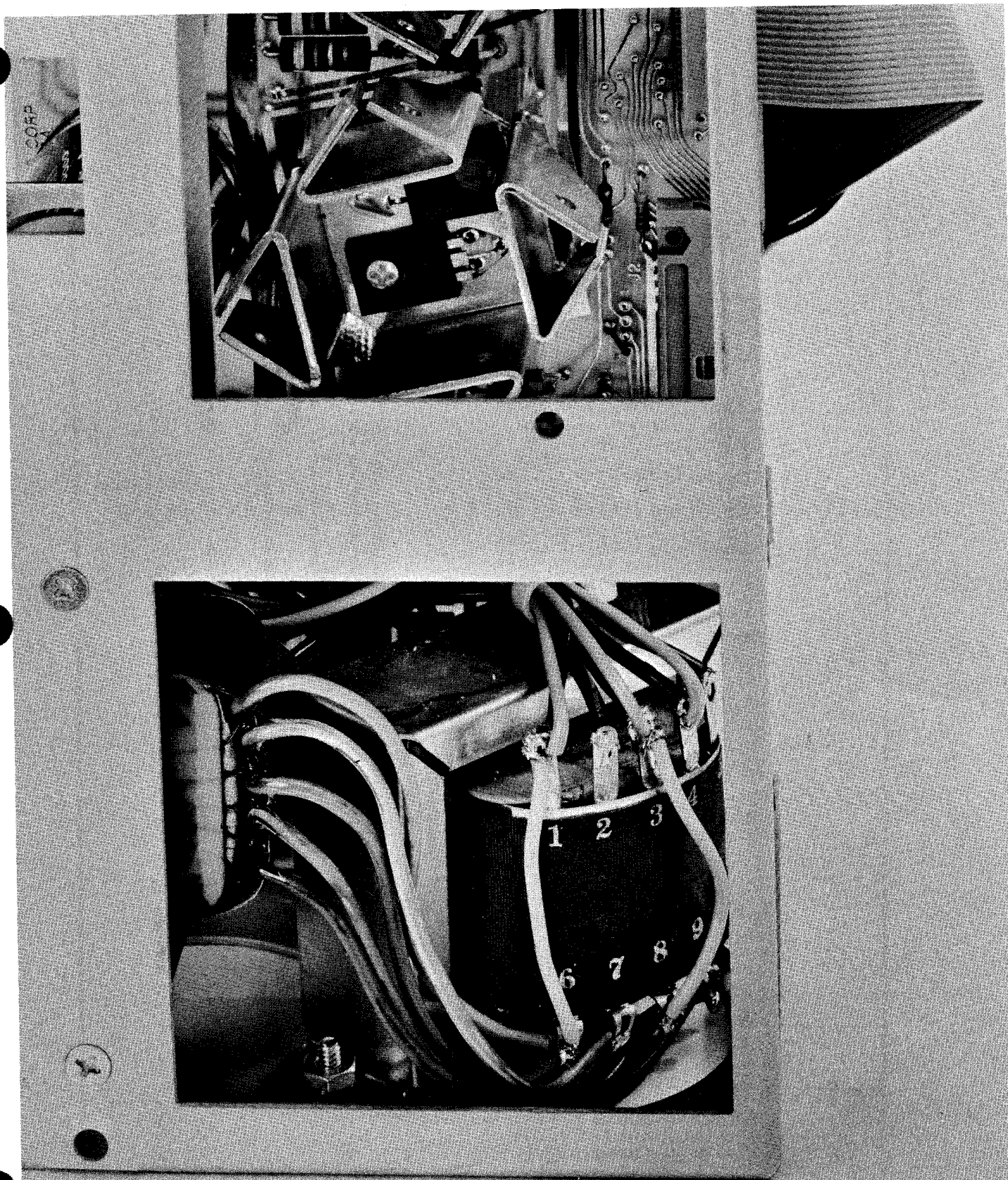
FPS-U REV.3
FIGURE 3
Chassis and Circuit Board Assembly -
Overall View



FPS-U REV.3
FIGURE 4
Circuit Board - Termination Resistor
and Diode Mounting

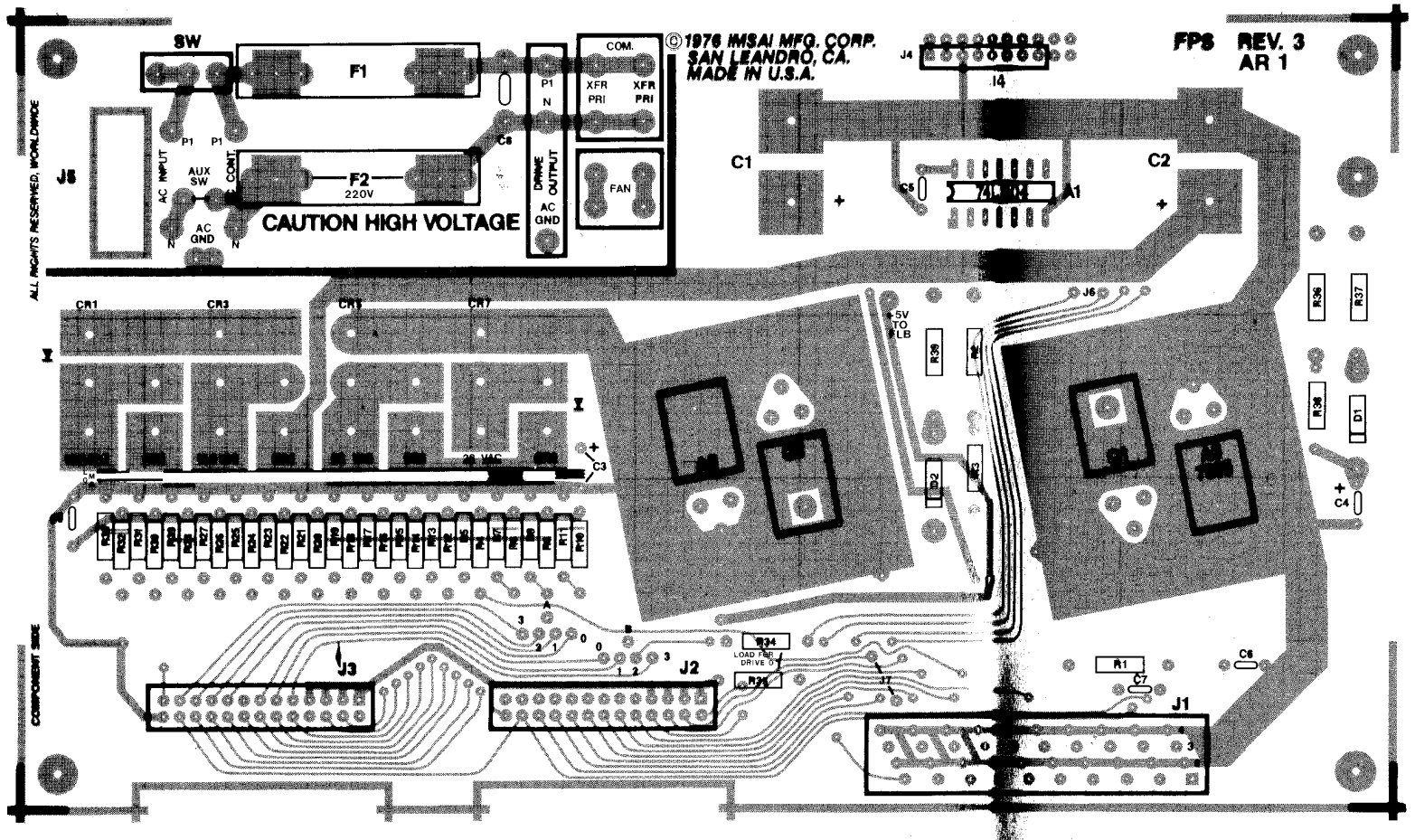


FPS-U REV.3
FIGURE 5
Circuit Board - Heatsink
and Regulator Mounting



FPS-U REV.3
FIGURE 6
Circuit Board - Transformer Mounting

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL REV. 0	3/76	
1	MOD TO FPS REV. 3	12/76	Pru

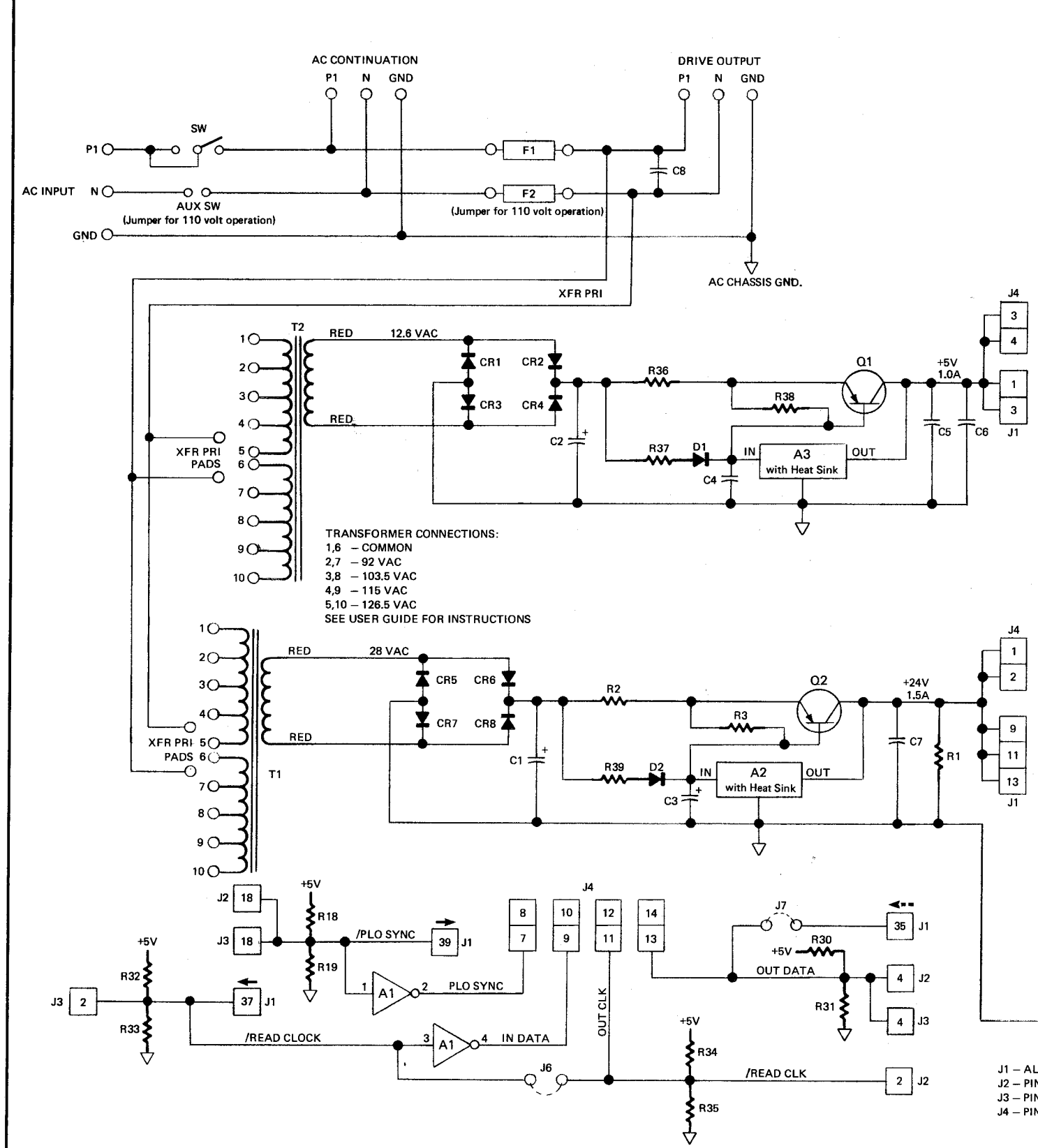


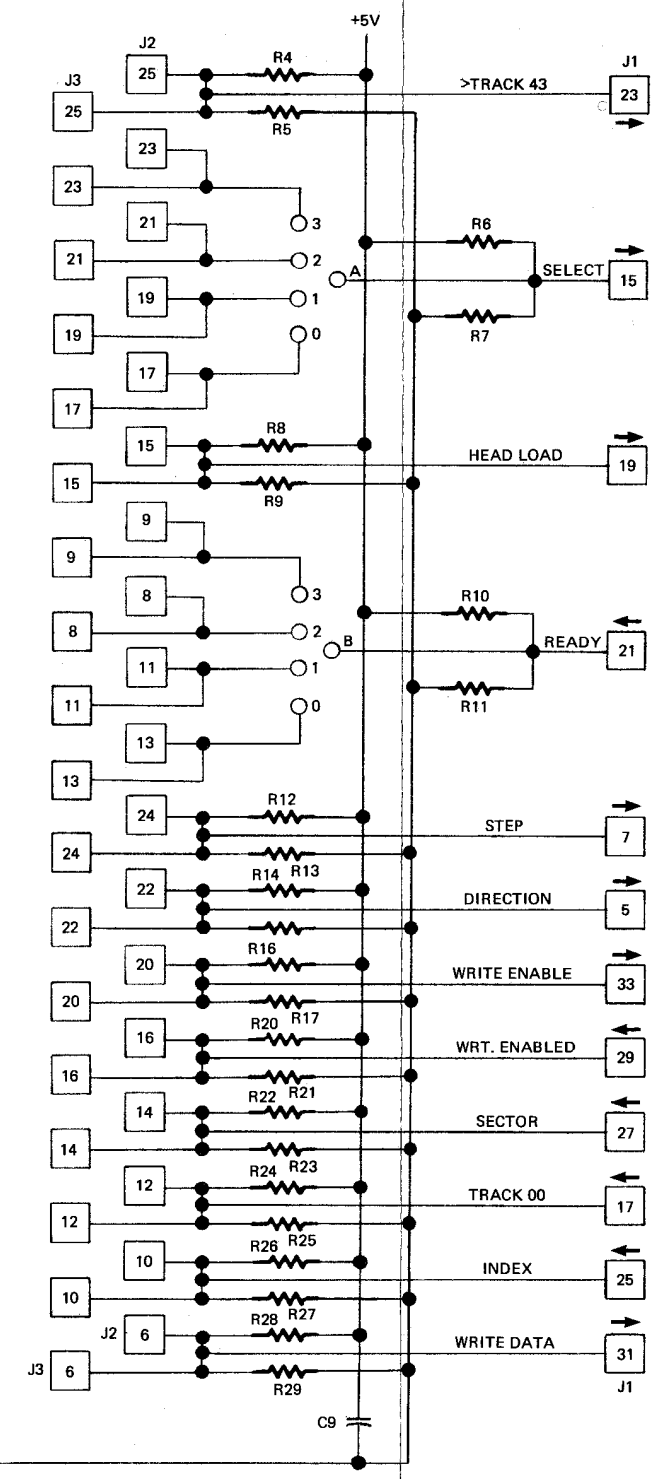
Notes:

Capacitor C1 is 4100 uF 50V.
Capacitor C2 is 5600 uF 25V.
Capacitor C3 & C4 are 2.2 uF 50V.
Capacitor C5 thru C7 & C9 are .1 uF.
Capacitor C8 is .02 uF 500 V.
Diodes are MR501.
Resistors are ¼ watt unless noted.
R1 is 2.2K ohm ½ watt.
R4, R6, R8, R12, R14, R16, R18 & R28 are 120 ohm ½ watt.
R5, R7, R9, R13, R15, R17, R19, & R29 are 220 ohm
R10, R20, R22, R24, R26, R30, R32 & R34 are 470 ohm.
R11, R21, R23, R25, R27, R31, R33 & R35 are 680 ohm.
R2, R36, R37 & R39 are .47 Ohm 2 watt.
R3 & R38 are 47 ohm.
Transistors are MJE2955K.
I.C. A2 is a 78HV24CU.
Fuses are AGC 2½ or 1½ A.
J1 is 40 Pin Header (on Cable Assembly).
J2 & J3 are 26 Pin Headers.
J4 is 8 Pin Connector
J5 is a Power Socket.
T1 is 117-28 VAC
T2 is 117-12.6 VAC

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC. ANGLES ± ± ±		
APPROVALS	DATE	FLOPPY DISK SYSTEM ASSEMBLY DIAGRAM FPS–U REV. 3 12/76
DRAWN PRU	12/14/76	
CHECKED D. Carroll	2/2/77	SCALE — / SIZE B / DRAWING NO. 91–2020001
		DO NOT SCALE DRAWING / SHEET

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL REV. 0	4/76	
1	MOD TO FPS-U REV. 3	12/76	





A1	74LS04
A2	78HV24CU
A3	7805
C1	4100 uF 50V
C2	5600 uF 25V
C3, C4	2.2 uF 50V
C5, C6, C7	.1 uF
C8	.02 uF 500V
C9	.1 uF
CR1 thru CR8, D1, D2	MR501
R1	2.2K ½W
R2	.62 2W
R3	47 ¼W
R4, R6, R8, R12, R14, R16, R18, R28	120 ¼W
R5, R7, R9, R13, R15, R17, R19, R29	220 ¼W
R10, R20, R22, R24, R26, R30, R32, R34	470 ¼W
R11, R21, R23, R25, R27, R31, R33, R35	680 ¼W
R36	.62 2W
R37	47 ¼W
R38	.62 2W
R39	
T1	117-28 VAC 2A
T2	117-12.6 VAC 2A
F1, F2	AGC 2½ or TWO 1½ A FUSE
	SEE USER GUIDE FOR WIRING INSTR.
J1	40 PIN HEADER
J2, J3	26 PIN CONNECTOR
J4	20 PIN CONNECTOR
J5	POWER SOCKET
J6, J7	DRIVE CONFIG. JUMPER
Q1	
Q2	

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS ± DEC ± ANGLES ±

SCHEMATIC DIAGRAM
FPS–U REV. 3 12/76

APPROVALS	DATE
DRAWN	12/15/76
CHECKED	12/15/76

SCALE —— SIZE C DRAWING NO. 91–3020001

DO NOT SCALE DRAWING SHEET 1 OF 1

BOARD: FLOPPY POWER SUPPLY

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
Solder	15-0000001	10'	
Heat Sink	16-0100007	2	Wakefield Heat Sink/690-220-B
Screw	20-3203001	4	#6x¼" Self-Tapping Sheet Metal
Screw	20-3406001	4	6-32x3/8" Phillips Flat Head Machine
Screw	20-3402001	4	6-32x3/8" Phillips Pan Head Machine
Screw	20-3701003	2	6-32x3/4" Round Head Machine, Nylon
Screw	20-4402001	2	8-32x3/8" Phillips Pan Head Machine
Screw	20-5201001	4	10-32x¼" Binding Head Machine
Nut	21-3120001	8	6-32 Hex Nut
Washer	21-3310001	4	#6 Flat Washer
Lockwasher	21-3350001	10	#6 Internal Star Lockwasher
Washer	21-3390001	1	#6 1/16x3/8" Flat, Fiber Washer
Lockwasher	21-4350001	2	#8 Internal Star Lockwasher
Lockwasher	21-5350001	4	#10 Internal Star Lockwasher
Header	23-0400012	2	26 Pin Header, SF 3429-1002
Wire	22-1018001	30"	18 GA., Stranded Wire, Orange
Wire	22-1018002	24"	18 GA., Stranded Wire, Yellow
Header	23-0400019	1	Header, AMP 87233-7 or AP Products 929648-01-8
Insulator	28-0100001	2	Insulator, Thermalloy 56-77-2AP
Transformer	29-0400002	1	Tranex 4-3914-1
Transformer	29-0400003	1	Tranex 4-3915-1
Resistor	30-2047664	4	.47 Ohm, 2 Watt/yellow, violet, silver

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
Resistor	30-2470362	2	47 Ohm, ¼ Watt/yellow, violet, black
Resistor	30-3120362	8	120 Ohm, ¼ Watt/brown, red, brown
Resistor	30-3220362	8	220 Ohm, ¼ Watt/red, red, brown
Resistor	30-3470362	8	470 Ohm, ¼ Watt/yellow, violet, brown
Resistor	30-3680362	8	680 Ohm, ¼ Watt/blue, grey, brown
Resistor	30-4220462	1	2.2K Ohm, ½ Watt/red, red, red
Capacitor	32-2002011	1	.02uF, 500V Disk Ceramic
Capacitor	32-2010010	4	.1uF Disk Ceramic
Capacitor	32-2202270	2	2.2uF, 50V Tantalum
Capacitor	32-2440060	1	4100uF, 50V Electrolytic
Capacitor	32-2450060	1	5600uF, 25V Electrolytic
Fuse	33-0100004	1	2.5 Amp, Fast Blow Fuse, AGC 2½
Fuse	33-0100005	2	1.5 Amp, Fast Blow Fuse, AGC 1½
Clip	33-0200001	4	Fuse Clip
Diode	35-1000003	10	MR501
Transistor	35-2000006	2	MJE 2955K
74LS04	36-0740402	1	Hex Inverter (Low Power Schottky)/SN74LS04N
7805	36-0780501	1	5V Positive Regulator/7805CU
78HV24	36-0782401	1	24V Positive Regulator/78HV24CU
Cable	91-0400013	1	Cable V Assembly
Cable	91-0400014	2	Cable X Assembly
Cable	91-0400015	1	Cable P Assembly
PC Board	92-0000009	1	FPS Rev. 3
Label	93-0000001	1	"Voltage and Hz"

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
Duct	93-3020020	1	Die-Cut Paper Duct Assembly
Chassis	93-4020009	1	Sheet Metal Chassis, FPS Rev. F

ASSEMBLY INSTRUCTIONS----------

GENERAL: The Component side of the Printed Circuit Board may be identified by the presence of the white silkscreen and the words, "FPS-U REV 3.2", in the upper right hand corner. All component locations referenced in the Assembly Instructions are given with respect to the Component Side of the Board.

( ) 0. Unpack and check all parts against the Parts List enclosed with the package.

RESISTOR INSTALLATION

( ) 1. Insert and solder the four 0.47 Ohm 2W Resistors, (yellow, violet, silver, gold), at locations R2, R36, R37, and R39 as shown on the Assembly Diagram.

( ) 2. Insert and solder the two 47 Ohm 1/4 Watt Resistors, (yellow, violet, black, gold), at locations R3, and R38 as shown on the Assembly Diagram.

( ) 3. Insert and solder the one 2.2K Ohm Resistor,(red,red, red,gold), at location R1 as shown on the Assembly Diagram.

( ) 4.

Insert and solder the remaining Resistors according to TABLE 2 and the Assembly Diagram.

TABLE 2 specifies which resistors are to be installed for a particular Drive Number. The column labelled, DRIVE 0, refers to the FPS-U of the first drive in a multiple drive system.

The column labelled, MIDDLE DRIVE, applies to the FPS-U of the second drive in a 3-drive system and the FPS-U of the second and third drives in a 4-drive system.

The column labelled, LAST DRIVE, applies to the FPS-U of the last drive in the Daisy Chain of a multiple drive system.

The column labelled, SINGLE DRIVE SYSTEM, applies to the FPS-U used in a one-drive system. Note that a SINGLE DRIVE system is a special case since it is both Drive 0 and the Last Drive. Therefore, the resistors indicated in TABLE 2, under the heading SINGLE DRIVE SYSTEM, include all Drive 0 and Last Drive resistors.

To simplify the installation of the Resistors shown in TABLE 2, the circuit board has been marked with identification guide lines. These lines are located above the resistor array on the left side of the board.

The Top identification line marked, "L", locates the resistor pairs for the LAST DRIVE. The following line marked, "M", locates the resistor pairs for the MIDDLE DRIVE(S). The next line marked, "0", locates the resistors for Drive 0. The bottom line marked, "P", locates the 120/220 OHM pairs where applicable (TABLE 2).

Figures 1 through 4 may be used as examples of correct component placement for each of the four types of drive configurations. Note that R34 and R35 are located to the right of connector J2 at the bottom of the board.

IC AND DIODE INSTALLATION

( ) 5.

Insert and solder one 74LS04 at location A1 as shown on the Assembly Diagram. Insure that pin 1 is oriented towards the upper left as indicated on the board silkscreen.

( ) 6.

Insert and solder two MR501 diodes at lo-cations D1 and D2 as shown on the Assembly Diagram. Insure that the diode band is oriented to match the marking on the board. To bend the leads of the diode, grip the lead to be bent next to the diode body with a pair of needlenose pliers and bend the free end into position. This will reduce the possibility of breaking the wirebond in the diode.

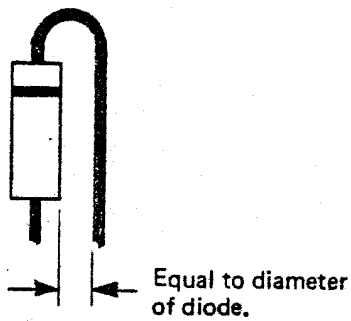
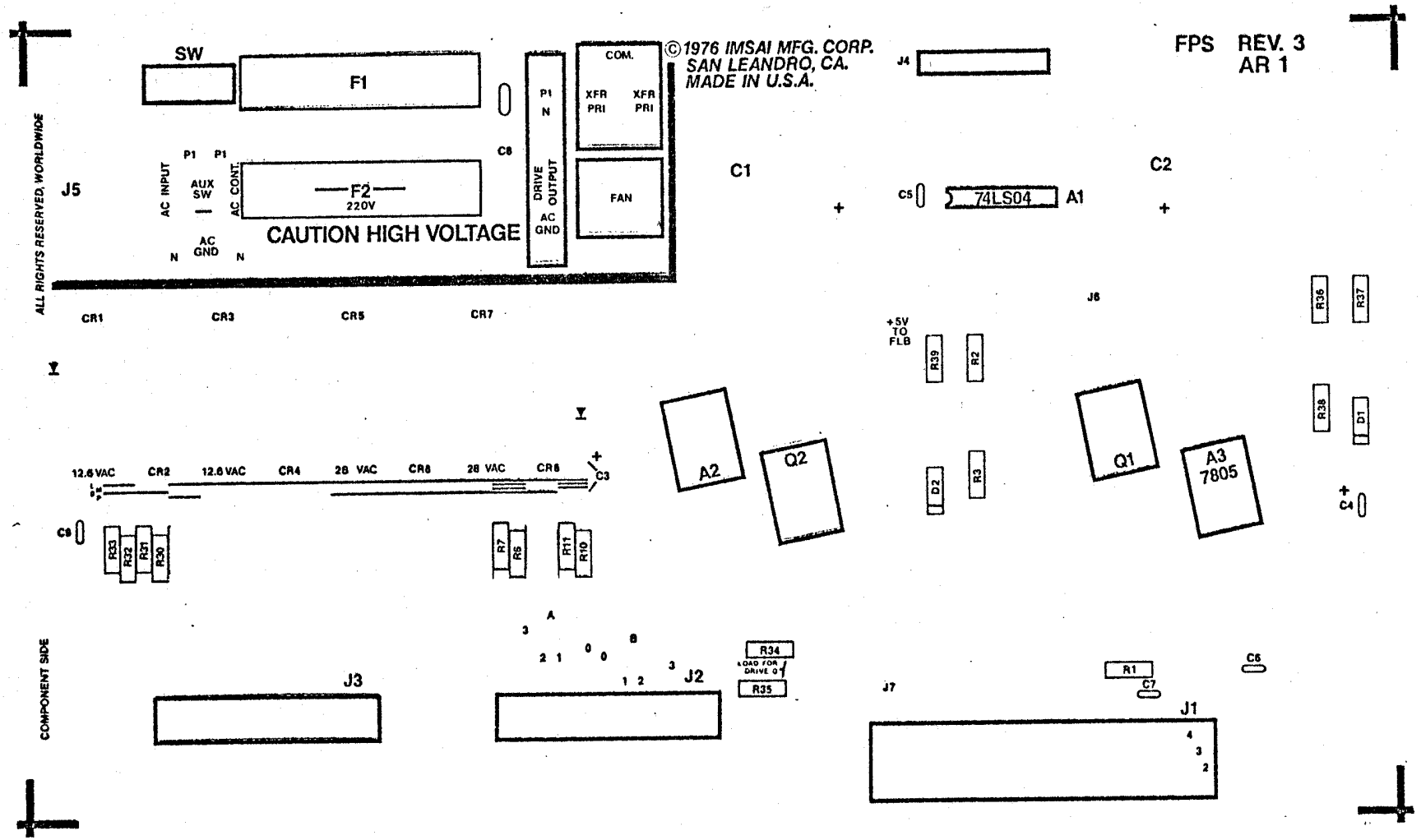


TABLE 2

LOCATION	RESISTOR VALUE	DRIVE 0	MIDDLE DRIVE	LAST DRIVE	SINGLE DRIVE SYSTEM
R29	220 Ohm, ¼ Watt(red, red, brown)			X	X
R19	" " "			X	X
R17	" " "			X	X
R15	" " "			X	X
R13	" " "			X	X
R5	" " "			X	X
R7	" " "	X	X	X	X
R9	" " "			X	X
R28	120 Ohm, ¼ Watt(brown, red, brown)			X	X
R18	" " "			X	X
R16	" " "			X	X
R14	" " "			X	X
R12	" " "			X	X
R4	" " "			X	X
R6	" " "	X	X	X	X
R8	" " "			X	X
R33	680 Ohm, ¼ Watt(blue, grey, brown)	X		X	X
R31	" " "	X			X
R27	" " "			X	X
R25	" " "			X	X
R23	" " "			X	X
R21	" " "			X	X

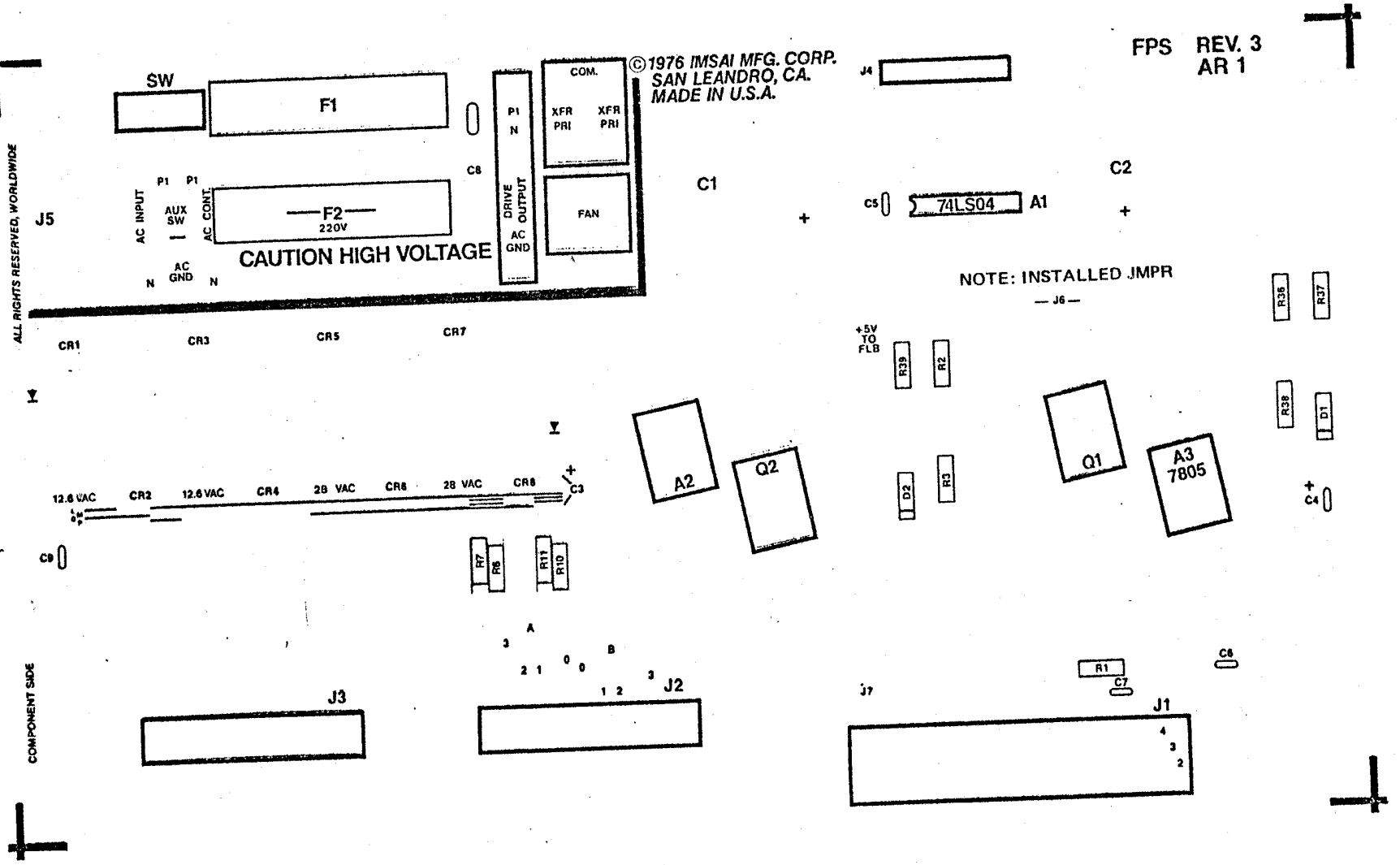
LOCATION	RESISTOR VALUE	DRIVE 0	MIDDLE DRIVE	LAST DRIVE	SINGLE DRIVE SYSTEM
R11	680 Ohm, ¼ Watt(blue, grey, brown)	X	X	X	X
R35	" " "	X			X
R32	470 Ohm, ¼ Watt(Yellow, violet, brown)	X		X	X
R30	" " "	X			X
R26	" " "			X	X
R24	" " "			X	X
R22	" " "			X	X
R20	" " "			X	X
R10	" " "	X	X	X	X
R34	" " "	X			X

Jumper J6 (Jumper J7 is not used) | | X | X |



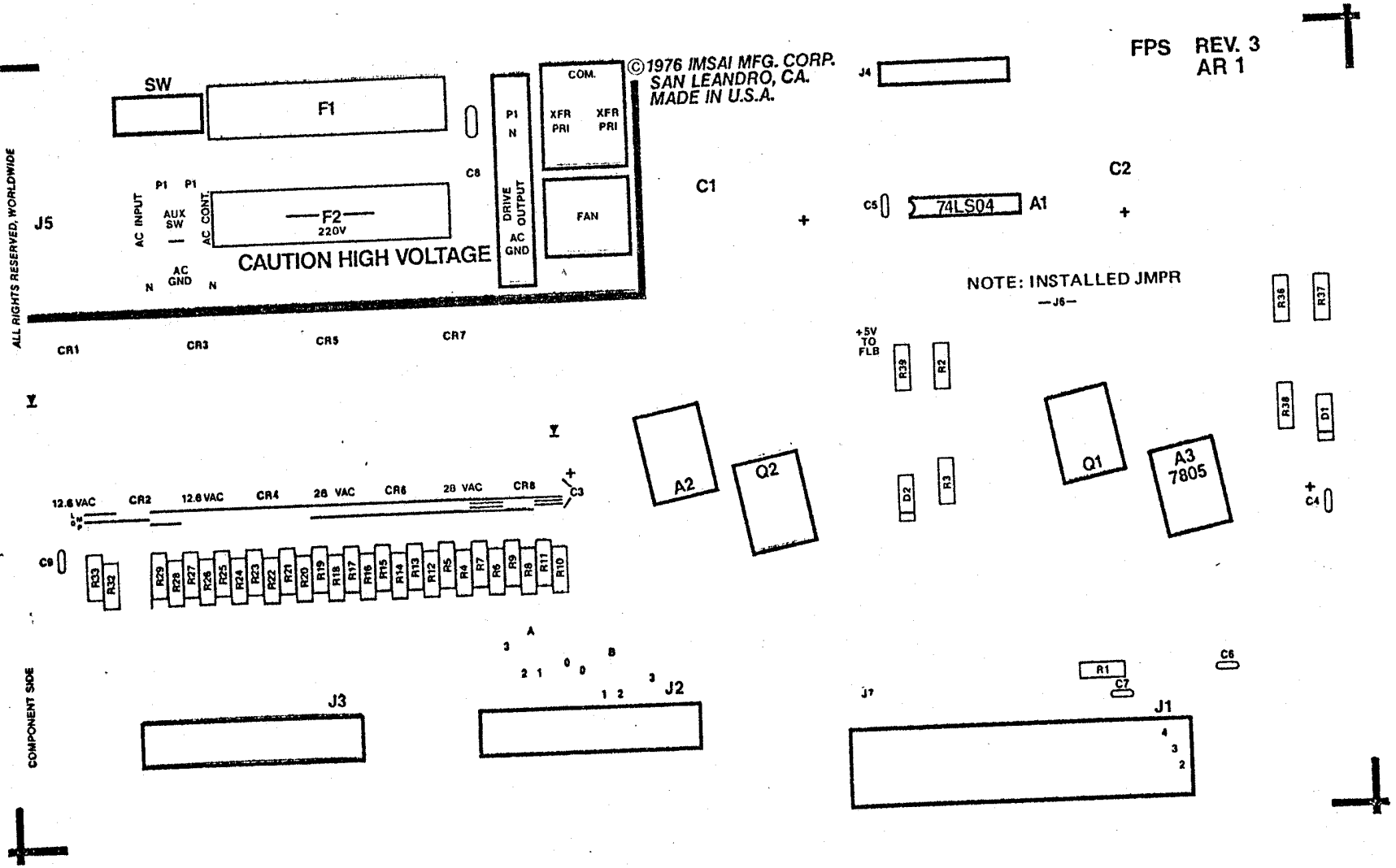
RESISTOR LISTING FIGURE 1

DRIVE 0 FPS REV. 3
MULTIPLE DRIVE SYSTEM



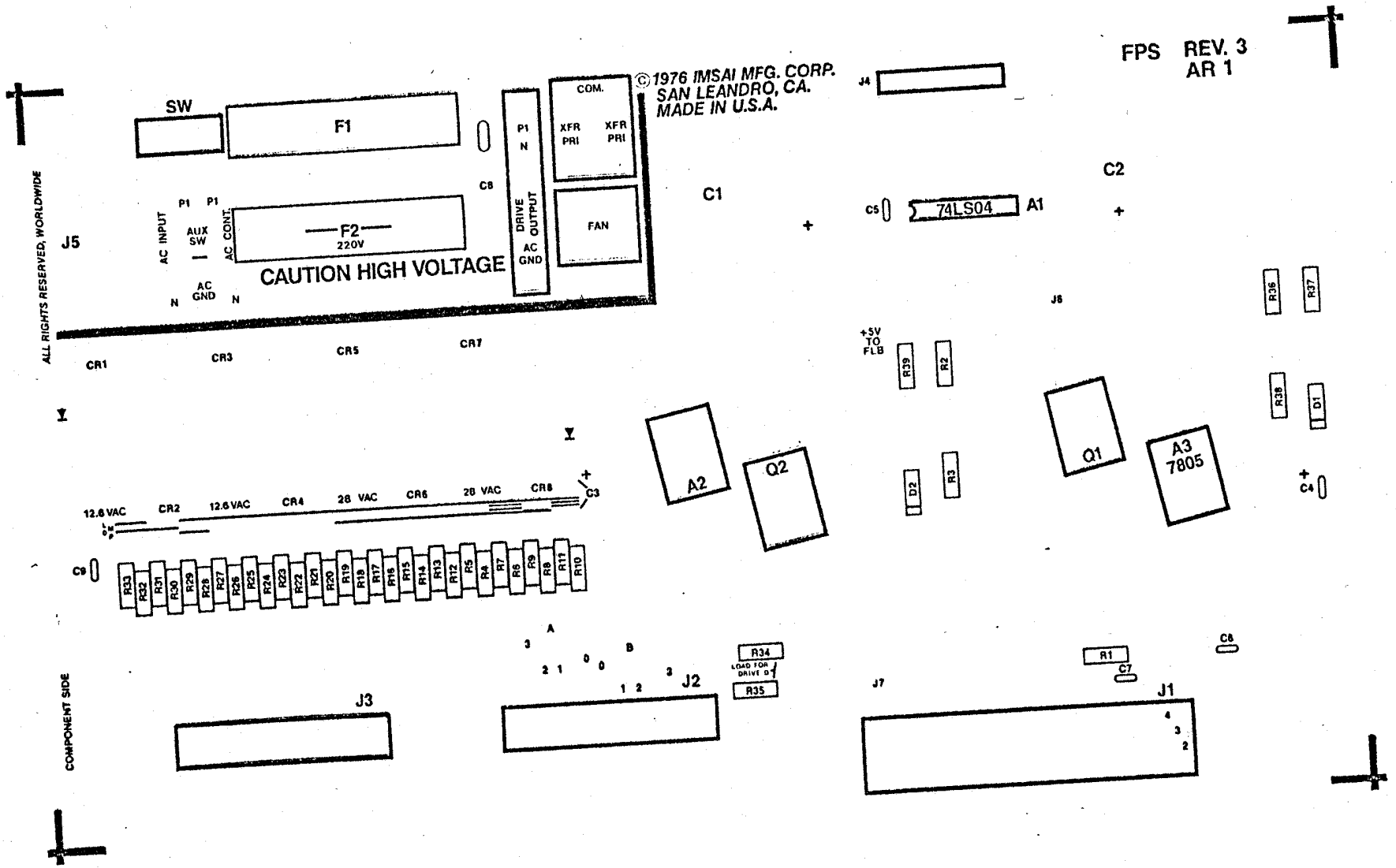
RESISTOR LISTING FIGURE 2

MIDDLE DRIVE FPS REV. 3
MULTIPLE DRIVE SYSTEM



RESISTOR LISTING FIGURE 3

LAST DRIVE FPS REV. 3
MULTIPLE DRIVE SYSTEM



RESISTOR LISTING FIGURE 4

SINGLE DRIVE SYSTEM

FPS REV. 3

( ) 7.

Insert and solder eight MR501 Diodes in positions CR1 through CR8 as shown on the Assembly Diagram. Form the Diode leads as shown in STEP 6, remembering to hold the lead to be bent next to the Diode body with a pair of needlenose pliers.

With the leads bent exactly as shown in STEP 6, mount each diode so that the body of the diode is over the appropriate top row mounting hole with the band on top. The remaining lead should be inserted into the appropriate lower row mounting hole.

CAPACITOR INSTALLATION

( ) 8.

Insert and solder two 2.2 uF, 50V, Tantalum capacitors in locations C3 and C4 as shown on the Assembly Diagram. Insure that the terminal marked, "+", is oriented to match the board marking, "+".

( ) 9.

Insert and solder four 0.1 uF disk ceramic capacitors in locations C5, C6, C7, and C9 as shown on the Assembly Diagram.

( ) 10.

Insert and solder one 0.02 uF, 500Volt, disk ceramic capacitor in position C8 as shown on the Assembly Diagram.

SIGNAL CONNECTOR INSTALLATION

( ) 11.

Locate and cut pin 26 on each of the two 26 pin connectors. To locate pin 26, hold the connector with the molded part number (NO.3429) on top and the CABLE CONNECTOR pins facing towards you. Pin 26 is now the last pin in the lower left hand corner. Note that pin ONE is marked with a molded triangle on the top right side of the connector. Once pin 26 has been located, cut it off flush with the connector body.

NOTE: The CABLE CONNECTOR pins are those which are recessed in the connector body, as opposed to the BOARD SOLDER pins which are not recessed. The cut must be made to CABLE CONNECTOR pin 26.

( ) 12.

Insert and solder the two 26 pin connectors at J2 and J3 as shown on the Assembly Diagram. Insure that CABLE CONNECTOR pins face OUTWARD from the edge of the board.

( ) 13.

Insert the 8 pin Right Angle Connector at location J4 as shown on the Assembly Diagram. The connector should be mounted on the SOLDER SIDE of the board with the long pins extending towards the upper edge of the board.

Before soldering, reference the board photos to insure that the connector is correctly oriented. Verify that the connector is inserted into the bottom row of mounting pads. When you are certain of correct placement, solder the connector in place.

NOTE: The board Photos incorrectly show J4 as a 7 pin connector. Also, the additional mounting pads to the side of J4 are not drilled on current boards.

( ) 14. Insert the 40 pin header that terminates one end of CABLE P into location J1 as shown on the Assembly Diagram. Orient the header on the COMPONENT SIDE of the board so that the cable extends off of the bottom of the board. Reference the board photos to verify the orientation. When you are certain that the placement is correct, solder the header into place.

FUSE INSTALLATION

( ) 15. Insert and solder two fuse clips in location F1 as shown on the Assembly Diagram. This may be done by snapping the clips onto the ends of the fuse and holding this assembly in place while soldering from the back of the board. For 200 volt range operation, solder two additional fuse clips in the location labelled Fuse 2.

JUMPER INSTALLATION

( ) 16. For 100 Volt Range Operation:
Using a component lead or a short length of wire, insert and solder a jumper between the two pads in location F2 as shown on the Assembly Diagram. Reference the board photos for verification.

( ) 17.

Using a component lead or a short length of wire, insert and solder a jumper between the two pads immediately below the board markings, "AUX SW", as shown on the Assembly Diagram. Reference the board photos for verification.

( ) 18.

If this FPS-U is to be used as the Second Drive in a cabinet, (ie. as Drive 1 or Drive 3), insert and solder a jumper between the two right-most pads in the board location marked, "SW".

NOTE: The board photos only show an FPS-U set up as the First Drive in a cabinet and thus do not indicate this jumper.

If this FPS-U is to be used as the First or Only Drive in a cabinet, first identify the half of CABLE AB which terminates in a Female Molex Connector. Insert the two wires of this cable into the board location ,"SW", using the two right-most pads. Verify that the wires are inserted from the component side of the board, and solder into place.

NOTE: The board photos show a switch mounted directly to the FPS-U board and do not reflect the proper use of CABLE AB.

POWER CABLE INSTALLATION

( ) 19.

Insert CABLE V into the board at location J5 as shown on the Assembly Diagram. Pass the three wires of CABLE V through the cutout in location J5 from the component side of the board. Orient the connector so that the pointed end is toward the top end of the board and push down on the connector until the mounting

ears lock into place.

( ) 20. Insert the three wires of connector J5 from the BACK of the board into the appropriate locations as follows:

Insert and solder the BLACK WIRE to the pad directly above the board location marked "AC INPUT". This pad is the left-most terminal marked "P1".

Insert and solder the WHITE WIRE to the pad directly below the board location marked "AC INPUT". This pad is the left-most terminal marked "N".

Insert and solder the GREEN WIRE to the left-most pad, directly below the board location marked, "AC GND".

( ) 21. Install one CABLE X by inserting the three CABLE X wires from the COMPONENT SIDE of the board into the appropriate locations as follows:

Insert and solder the BLACK WIRE into the pad directly above the board markings, "AC CONT".

Insert and solder the WHITE WIRE to the pad directly below the board markings "AC CONT". This pad is the right-most terminal marked "N".

Insert and solder the GREEN WIRE to the remaining pad directly below the board marking "AC GND".

NOTE: The board photos do not show this Cable X.

( ) 22. Install the remaining CABLE X by inserting the three CABLE X wires from the COMPONENT SIDE of the board into the board location marked, "DRIVE OUTPUT", as follows:

Insert and solder the BLACK WIRE to the pad marked "P1" (top) in the board location marked "DRIVE OUTPUT".

Insert and solder the WHITE WIRE to the pad marked "N" (middle) in the board location marked "DRIVE OUTPUT".

Insert and solder the GREEN WIRE to the pad marked "AC GND" (bottom) in the board location marked "DRIVE OUTPUT".

REGULATOR AND HEAT SINK INSTALLATION

( ) 23.

Bend the leads of the two MJE 2955K Pass Transistors at 90 degree angles from the mounting plane of the device. The bends should be made down, away from the side bearing the Device Number and should allow the device to be aligned so that the mounting hole and the leads line up with the corresponding hole and pads at board locations Q2 and Q1. When the bends have been made, set the two devices aside.

NOTE: One way to accomplish this is to place the lettered side of the device FACE DOWN against the board at location Q1 or Q2. Align the device so that the mounting hole is centered and the three device leads cross directly over the lead solder pads. While holding the body of the device firmly in place, carefully bend each lead at a 90 degree angle, up away from the board with a pair of needlenose pliers. Each bend must be made so that the axis of a bent lead coincides with the axis drawn through the appropriate board mounting pad.

( ) 24.

Bend the leads of one 7805 and one 7824 regulator at 90 degree angles from the mounting plane of the device. The bends should be made away from the side bearing

the Device Number and should allow the device to be aligned so that the mounting hole and the leads line up with the corresponding hole and pads at board locations A2 (for the 7824) and A3 (for the 7805). When the bends have been made, set the two devices aside.

NOTE: This may be accomplished by following the procedure outlined in the NOTE of step 23, using locations A2 (7824) and A3 (7805) for alignment.

( ) 25. Place and align one heat sink at the location surrounding Q2 as shown on the Assembly Diagram. Then place one pregreased insulating washer on the heat sink at location Q2. Align this washer so that it extends from the mounting hole on the board towards the triangle cutout in the heat sink where Q2 will mount.

( ) 26. Insert one MJE 2955K at location Q2 as shown on the Assembly Diagram. Insert one NYLON SCREW from the top of the board, through the mounting holes, and fasten from the bottom of the board with one lockwasher and one nut.

Verify that none of the leads of the device touch the heat sink. If alignment is correct, solder the leads of the device in place.

NOTE: The part number for Q2 (MJE 2955K) is incorrectly shown in the board photograph.

( ) 27.

Insert one 7824 at location A2 as shown on the Assembly Diagram. Then insert one 6-32 x 3/8 " pan head screw through the mounting hole from the top of the board. Place one FIBRE WASHER on the shaft of the screw from the back of the board and fasten in place with one #6 lockwasher and one nut. Verify that none of the leads of the device touch the heatsink. If alignment is correct, solder the leads of the device in place.

( ) 28.

Place and align one heat sink at the location surrounding Q1 as shown on the Assembly Diagram . Then place one pregreased insulating washer on the heat sink at location Q1. Align this washer so that it extends from the mounting hole on the board towards the triangle cutout in the heat sink where Q1 will mount.

( ) 29.

Insert one MJE 2955K at location Q1 as shown on the Assembly Diagram. Insert one NYLON SCREW from the top of the board through the mounting holes, and fasten from the bottom of the board with one lockwasher and one nut. Verify that none of the leads of the device touch the heat sink. If alignment is correct, solder the leads of the device in place.

NOTE: The part number for Q1 (MJE 2955K) is incorrectly shown in the board photos.

( ) 30.

Insert one 7805 at location A3 as shown on the Assembly Diagram . Then insert one 6-32 x 3/8 " pan head screw through the mounting hole from the top of the board. Fasten in place with one #6

lockwasher and one nut. Verify that none of the leads of the device touch the heat sink. If alignment is correct, solder the leads of the device in place.

FILTER CAPACITOR INSTALLATION

( ) 31.

Mount one 4100 uF , 50 volt, electrolytic filter capacitor at location C1 as shown on the Assembly Diagram. MAKE CERTAIN that the "+" terminal of the capacitor aligns with the "+" marking on the board. When the orientation is correct, fasten the capacitor in place with the two terminal screws and lockwashers.

( ) 32.

Mount one 5600 uF, 25 volt, electrolytic filter capacitor at location C2 as shown on the Assembly Diagram. MAKE CERTAIN that the "+" terminal of the capacitor aligns with the "+" marking on the board. When the orientation is correct, fasten the capacitor in place with the two terminal screws and lockwashers.

TRANSFORMER INSTALLATION

( ) 33.

Cut the primary leads numbered 1 through 5 from the 12.6 VAC transformer to a length of 3 3/4"; and strip 1/4" of insulation from the end of each lead.

NOTE: If the primary leads of the 12.6 VAC transformer are not labelled, they may be identified as follows: Leads 1 through 5 are located in the upper row with lead 1 on the far left; leads 6 through 10 are located in the lower row with lead 6 on the far left.

( ) 34.

Cut the primary leads numbered 6 through 10 from the 12.6 VAC transformer to a length of 4 3/4"; and strip 1/4" of insulation from the end of each lead.

NOTE: When making the transformer connections, use the photographs, wiring charts and Table 3 as references.

( ) 35.

Make the following 10 connections by crimping the appropriate wires in place. Do not solder at this time.

a) Connect lead #1 from the 12.6 VAC transformer to terminal #1 on the 28 VAC transformer.

b) Connect Lead #2 from the 12.6 VAC transformer to terminal #2 on the 28 VAC transformer.

c) Connect lead #3 from the 12.6 VAC transformer to terminal #3 on the 28 VAC transformer.

d) Connect lead #4 from the 12.6 VAC transformer to terminal #4 on the 28 VAC transformer.

e) Connect lead #5 from the 12.6 VAC transformer to terminal #5 on the 28 VAC transformer.

f) Connect leads 6 through 10 in the same manner (ie, lead #6 to terminal #6; lead #7 to terminal #7; etc.).

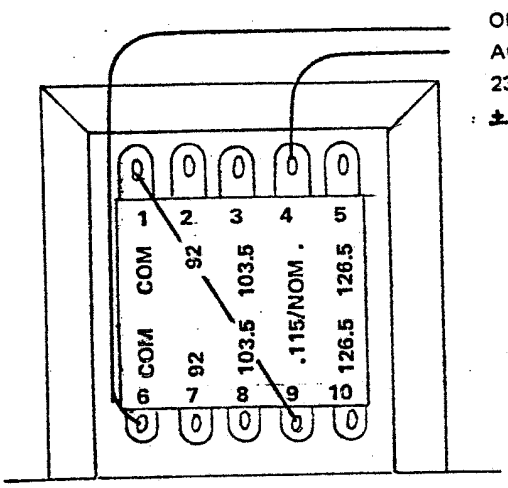
( ) 36.

Connect either one or two 2" lengths of 18 gauge wire (orange) between the appropriate primary terminals of the 28 VAC transformer. This is indicated in Table 3 under the column labelled "Strip These Lugs" and is also shown in the wiring charts.

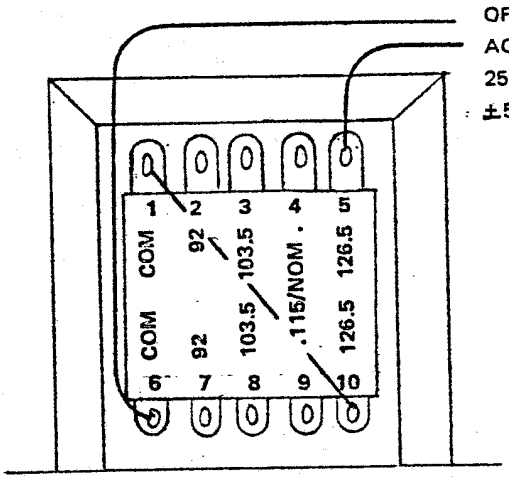
TABLE 3

INPUT AC CONNECTIONS FOR THE 28 VAC TRANSFORMER

FPS-U MODEL	CALCOMP DRIVE # VAC REQUIRED	TRANSFORMER TERMINAL INPUT VAC INPUTS ±5%	STRAP THESE LUGS	INPUT WIRES CONNECT TO THESE LUGS
100/60	140-005 100 VAC, 60 HZ	103 VAC	1 to 6 3 to 8	1 and 3
100/50	140B-004 100 VAC, 50 HZ	103 VAC	1 to 6 3 to 8	1 and 3
208/60	140-006 208 VAC, 60 HZ	207 VAC	1 to 8	6 and 3
208/50	140B-005 208 VAC, 50 HZ	207 VAC	1 to 8	6 and 3
220/50	140B-005 220 VAC, 50 HZ	230 VAC	1 to 9	6 and 4
230/60	140-002 230 VAC, 60 HZ	230 VAC	1 to 9	6 and 4
240/50	140B-006 240 VAC, 50 HZ	253 VAC	1 to 10	6 and 5

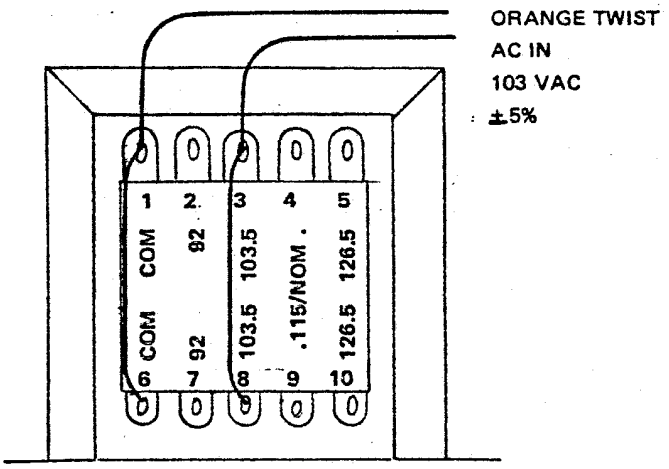


FRONT VIEW
FPS–U 230/60
FPS–U 220/50

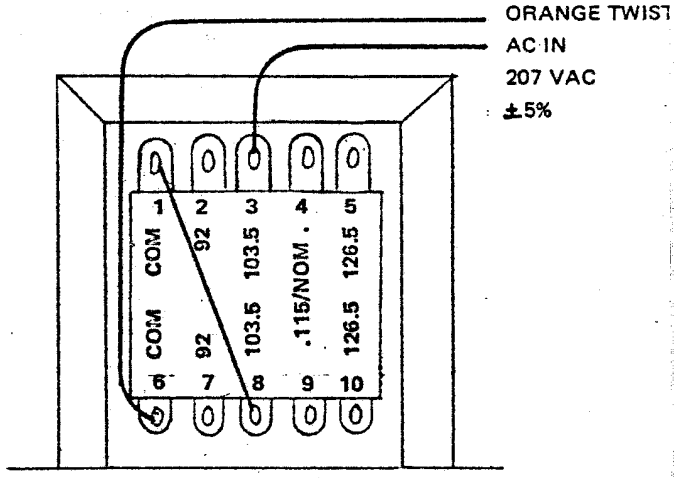


FRONT VIEW
FPS–U 240/50

WIRING CHART: 220 – 253 VAC; 50/60 HZ IN
See User Guide for more information. Use 2½A fuse.

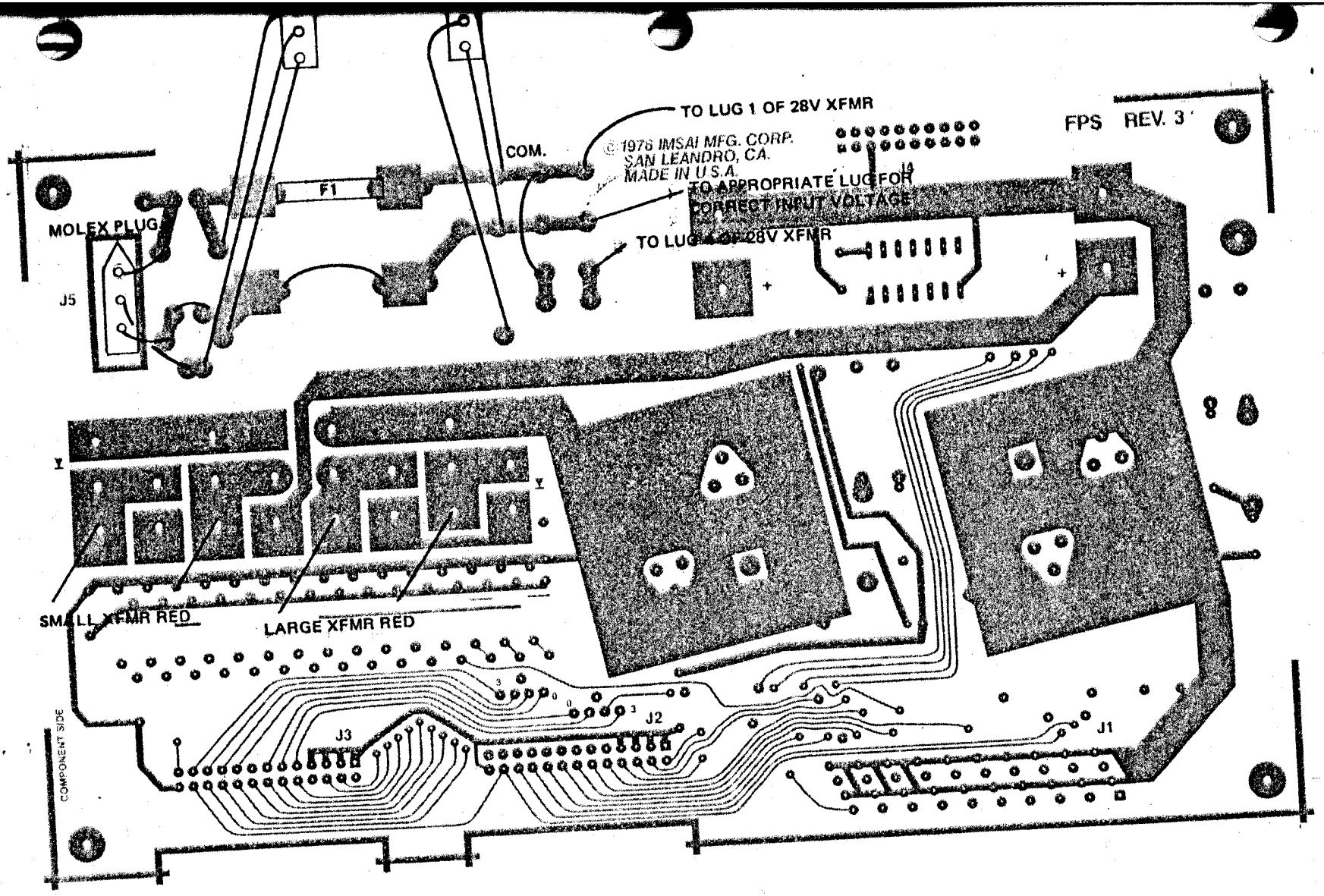


FRONT VIEW
FPS–U 100/60
FPS–U 100/50



FRONT VIEW
FPS–U 208/60
FPS–U 208/50

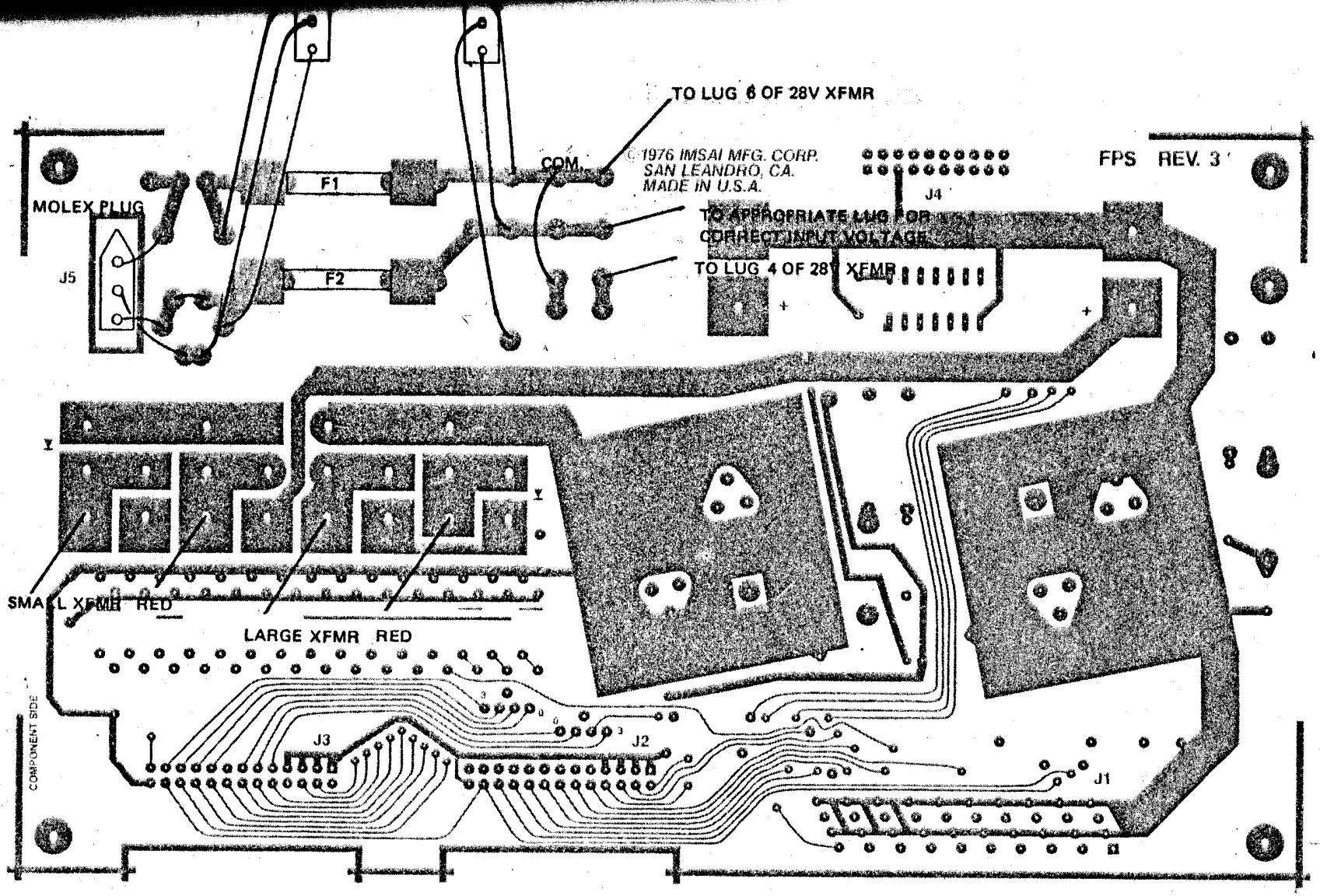
WIRING CHART: 103 – 207 VAC; 50/60 HZ IN
See User Guide for more information.



FPS-U REV. 3

100 VOLT RANGE OPERATION

WIRING CONNECTIONS



FPS-U REV. 3

200 VOLT RANGE OPERATION

WIRING CONNECTIONS

( ) 37. Orient the FPS-U chassis on its end so that the large rectangular opening is at the bottom with the interior area facing toward you. Mount one T117-12.6 transformer (the smaller of the two) on the lower right side of the large rectangular opening as shown in the FPS-U photographs. Insert the #6 flathead counter sunk screws through the transformer mounting holes from the outside of the chassis and fasten each screw in place with a flat washer, lockwasher and nut.

( ) 38 Mount one T117-28 transformer on the bottom end of the chassis; skewed in front of the large rectangular opening as shown in the FPS-U photographs. Insert two #6 flathead counter sunk screws through the transformer mounting holes from the outside of the chassis. Fasten each screw in place with a flat washer, lockwasher and nut.

( ) 39 Cut two 7" lengths of 18 gauge stranded wire (orange) and strip 1/4" of insulation from each end.

( ) 40. Take one 7" length of 18 gauge wire and connect one end to the "COM" pad (top) in the left-most board location labelled "XFR PRI". Solder this connection in place. Crimp the remaining end of this wire to the appropriate primary terminal fo the 28 VAC transformer. This will be terminal 1 for operation in the 100 volt range; or terminal 6 for operation in the 200 volt range (Table 3).

( ) 41. Take the remaining 7" length of 18 gauge wire and connect one end to the bottom

pad in the left-most board location labelled "XFR PRI". Solder this connection in place. Crimp the remaining end of this wire to the appropriate primary terminal of the 28 VAC transformer. This will be terminal 3, 4, or 5, as indicated in Table 3. Under the column "Input Wires Connect to These Lugs". NOTE: The two AC input wires should be twisted together to avoid line noise problems.

( ) 42

Crimp one end of a 7" length of 18 gauge wire (yellow) to primary terminal #4 of the 28 VAC transformer. Connect the other end of this wire to the left-most pad in the board area labelled "Fan". Solder this connection in place.

( ) 43.

Connect and solder one end of a 3" length of 18 gauge wire (yellow) wire to the right-most pad in the board area labelled "fan". Connect and solder the remaining end of this wire to the "COM" pad (top) in the right-most board location labelled "XFR PRI".

( ) 44.

Solder all primary terminal connections (terminal 1 through 10) on the 28 VAC transformer.

( ) 45.

Connect the two secondary wires from the 12.6 VAC transformer to the two pads labelled "12.6 VAC". These are located below diodes CR1 and CR3. Do not worry about polarity.

( ) 46.

Connect the two secondary wires from the 28 VAC transformer to the two pads labelled "28 VAC". These are located below diodes CR5 and CR7. Do not worry

about polarity.

MOUNTING THE FPS-U CHASSIS AND AIR DUCT

( ) 47. Fold the cardboard duct as shown in FIGURE 1 (in the Floppy Disk Cabinet section).

( ) 48. Insert the duct into the FPS-U Chassis from the rear, bending as necessary to get it into place as shown in FIGURE 3 (in the Floppy Disk Cabinet section).

( ) 49. Mount the FPS-U chassis to the rear of the Floppy Disk Drive with two 6-32 screws and two 8-32 screws. Tear off the two side tabs of the duct which extend beyond the sides of the FPS-U and Drive.

JUMPER SELECTION

( ) 50. Determine the Drive Number to be assigned to this Floppy Disk Drive (0 to 3).

NOTE: The selected Drive Number must be compatible with the type of Drive which was chosen in STEP 4 to insure that the proper termination resistors are present.

( ) 51. Locate the two Jumper Areas labelled "A" and "B" directly above connector J2. These areas may be identified as follows: Each jumper area consists of a line of 4 pads labelled 0-3, and a single pad centered directly above this row labelled "A" or "B".

( ) 52.

Connect a short jumper between the pad labelled "A" and the pad labelled with the selected drive number (0 to 3). Verify that the jumpr does not short to any adjacent traces or pads.

( ) 53.

In the second Jumper Area, connect a short jumper between the pad labelled "B" and the pad labelled with the selected drive number (0 to 3). Verify that the jumper does not short to any adjacent traces or pads.

( ) 54.

If the FPS-U is to be used with Drive 0, leave Jumpers J6 and J7 OPEN.

If the FPS-U is to be used with a drive other than Drive 0, connect a wire between the jumper pads at location J6, as shown on the Assembly Diagram. Leave J7 OPEN.

FINAL ASSEMBLY

( ) 55.

Plug the Molex Connector of the CABLE X which is connected to the Board Location marked "DRIVE OUTPUT", to the Molex receptacle on the rear of the Floppy Disk Drive through the opening provided. This opening is located on the FPS-U Chassis between the two filter capacitor mounting braces.

( ) 56.

Plug the 40 pin connector of CABLE P (J1) into the 40 pin receptacle on the rear of the Floppy Disk Drive.

( ) 57. Fasten the FPS-U PC board to the FPS-U chassis using the four #6 x 1/4" self-tapping screws.

( ) 58. Assembly of the Universal Floppy Power Supply is now complete.

USER GUIDE----------

AC INPUT POWER: AC input power to the board is made through the connector located at J5. If the FPS-U is used with the First or only drive in a cabinet, the AC source for J5 will be the AC linecord. If the FPS-U is used with the second drive in a cabinet, the AC source for J5 will be the CABLE X coming from the first drive's FPS-U at the board location "AC CONT".

POWER SWITCH: The FPS-U may be used in a switched or unswitched mode. If the FPS-U is used with the first or only floppy drive in a cabinet, one half of CABLE AB will connect to the right-most pads in the board area marked "SW". The other half of CABLE AB will connect to a switch on the rear of the floppy cabinet, providing ON/OFF switching for the AC power.

If the FPS-U is used as the second drive in a cabinet, a jumper is connected between the right-most pads in the board area marked "SW", and ON/OFF switching is accomplished from the Power Switch connected to the first drive.

FUSE: For use at 100 VAC, a 2.5 Amp fuse (3AG) is inserted in the fuse holder on the hot side of the AC line. For use at 200 VAC, a 1.5 Amp fuse is used at locations F1 and F2.

SELECTION OF DRIVE NUMBER: Selection of the floppy disk drive number is accomplished through the use of the two jumper areas labelled "A" and "B". The first jumper is connected between Terminal "A" and the appropriate pad in the row below which is marked with the selected drive number. The second jumper is connected between Terminal "B" and the appropriate pad in the row

below which is marked with the selected drive number.

NOTE: The selected drive number also determines which termination resistors are to be installed on the FPS-U Board.

TERMINATION RESISTORS: The correct termination resistors for a particular FPS-U are specified in the resistor selection TABLE 2 (Assembly Instructions).

The column labelled DRIVE 0, specifies the termination resistors used with the first drive in a multiple drive system. The column labelled MIDDLE DRIVE, specifies the termination resistors used with Drive 2 in a three drive system, or Drives 2 and 3 in a four drive system. The column labelled LAST DRIVE, specifies the termination resistors used with the Last Drive in the daisy chain of a multiple drive system. The column labelled SINGLE DRIVE SYSTEM, specifies the termination resistors used in a system composed of only 1 drive. It is a special case since a single drive is both the first and last drive in the system.

PLO BUS SIGNALS: A single PLO Board will support up to 4 drives in the daisy chain. J4 of the FPS-U used with Drive 0 will connect the PLO signals with the 26-pin signal bus. In addition, Jumper J6 must be jumpered across on the FPS-U of ALL DRIVES EXCEPT DRIVE 0. J7 is ALWAYS left OPEN.

FLOPPY DRIVE CABLE CONNECTIONS: The FPS-U provides for two cable connections to the Floppy Disk Drive. CABLE P at location J1, is a 40-pin DC signal cable to the Drive. It mates with the 40-pin connector located at the rear of the floppy disk drive; and connects the 26-pin signal bus to the floppy drive.

CABLE X from the FPS-U location "DRIVE OUTPUT", is a 3-pin Molex connector which supplies the +24 VDC to the Drive. It mates with the 3-pin Molex connector at the rear of the floppy disk drive.

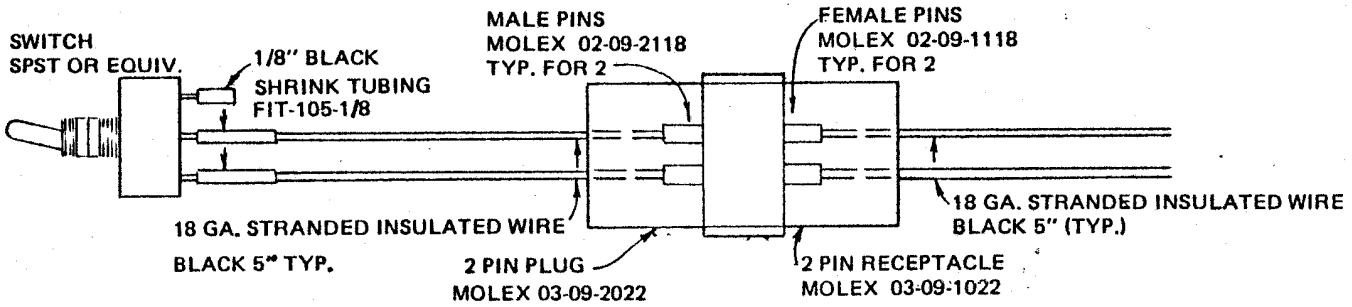
EXTERNAL CABLE CONNECTIONS: External cable connections to the floppy power supply provide for 1) the daisy chain in a multiple drive system; and 2) the data link from the computer.

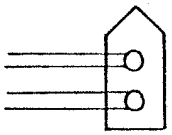
The cable connected to J2, of the FPS-U used with Drive 0, terminates at the Floppy Light Board, and a 25-pin EIA D Type connector. This connector will always mate with the cable coming from the computer.

The remaining connections serve to establish the daisy chain for the remaining drives in a multiple drive system. J3 of Drive 0 FPS-U will connect to J2 of Drive 1 FPS-U. J2 of Drive 1 FPS-U will connect to J2 of Drive 2 FPS-U. J3 of Drive 2 FPS-U will connect to J2 of Drive 3 FPS-U.

When making these connections, insure that all pin 1's are matched on the connectors and cables. DO NOT FORCE the connectors into place, as they are polarized to fit correctly only in their proper mounting position.

0	ORIGINAL	2/1/77	PRU

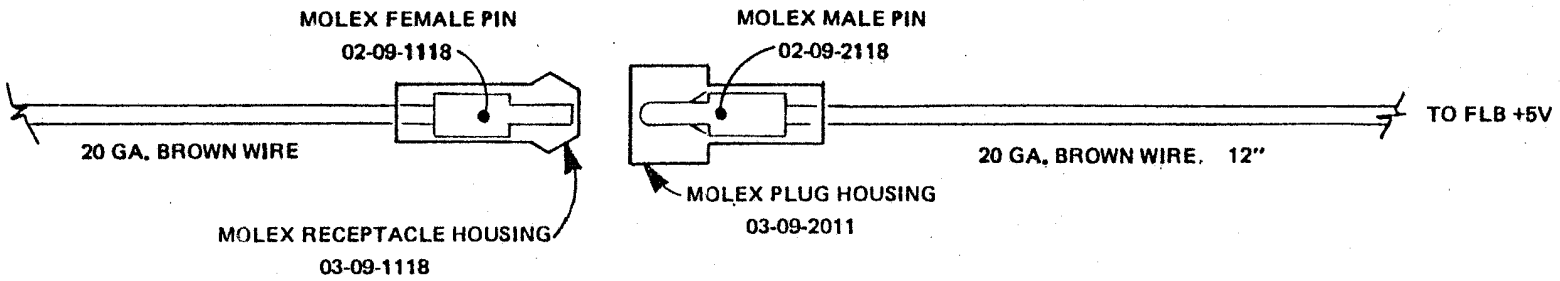




WIRE CONNECTION
FRONT VIEW

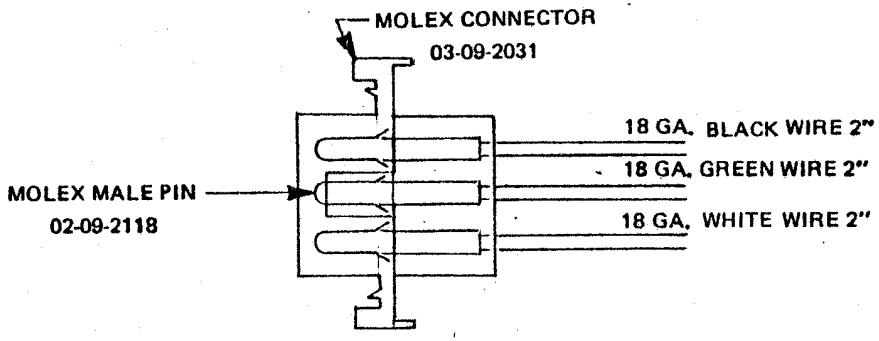
TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		IMSAI MFG. CORP. SAN LEANDRO, CA.		
APPROVALS	DATE	FLOPPY DISK SYSTEM CABLE AB ASSEMBLY 91-0400024		
DRAWN PRU	2/1/77			
CHECKED D. Carroll	2/2/77	SCALE	SIZE	DRAWING NO. 91-1040024
		DO NOT SCALE DRAWING		SHEET

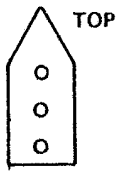
LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL	9/76	PRU



TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		
APPROVALS / DATE	FLOPPY DISK SYSTEM CABLE Q ASSEMBLY 91-0400019	
DRAWN PRU / 9/22/76	SCALE ——	SIZE / DRAWING NO. 91-1040019
CHECKED D. Carroll / 2/2/77	DO NOT SCALE DRAWING	SHEET

LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL	9/76	PRU

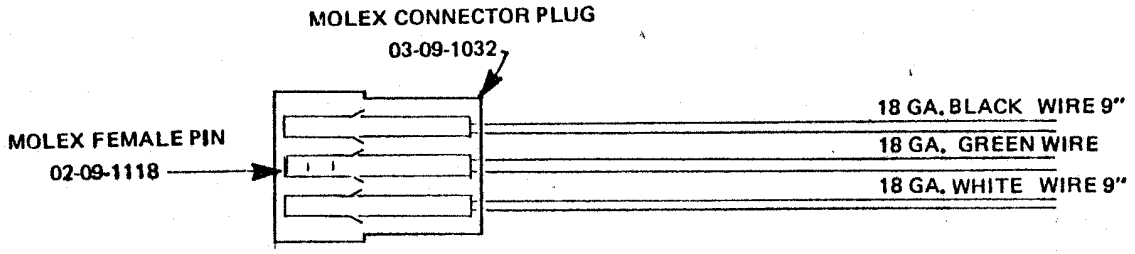


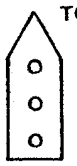


CONNECTOR DETAIL

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±	
APPROVALS / DATE	FLOPPY DISK SYSTEM CABLE V ASSEMBLY 91-0400013
DRAWN PRU 9/22/76	SCALE ——— SIZE DRAWING NO. 91-1040013
CHECKED D. Carroll 1/2/77	DO NOT SCALE DRAWING SHEET

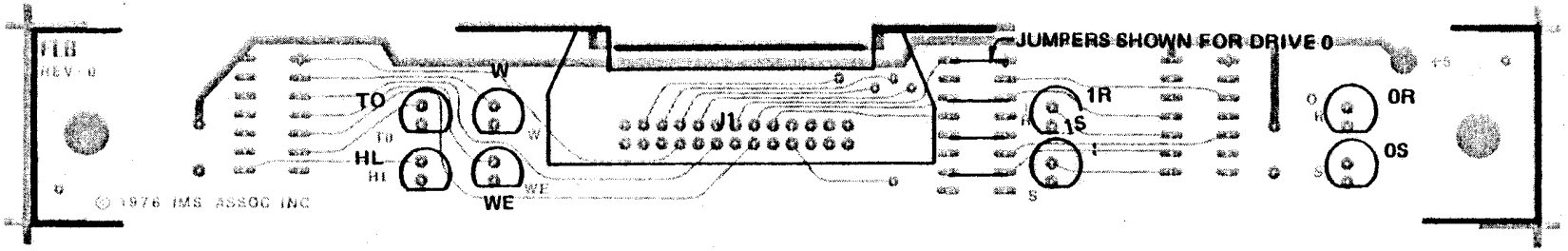
LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL	9/76	PRU



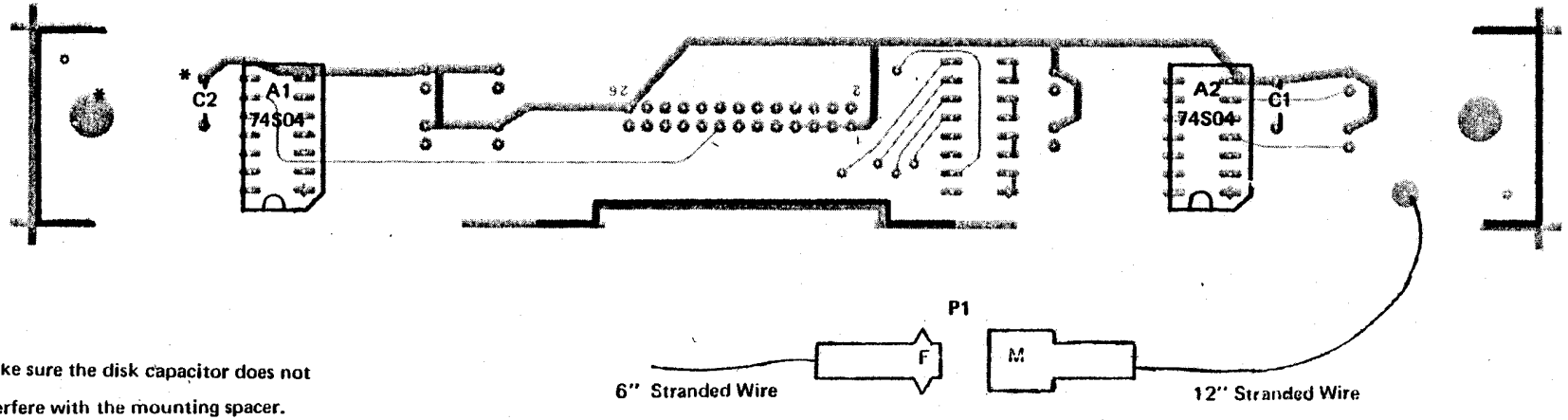


CONNECTOR DETAIL

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±	
APPROVALS / DATE	FLOPPY DISK SYSTEM CABLE X ASSEMBLY 91-0400014
DRAWN PRU 9/22/76	SCALE —— SIZE DRAWING NO. 91-1040014
CHECKED D. Cornell 1/3/77	
	DO NOT SCALE DRAWING SHEET



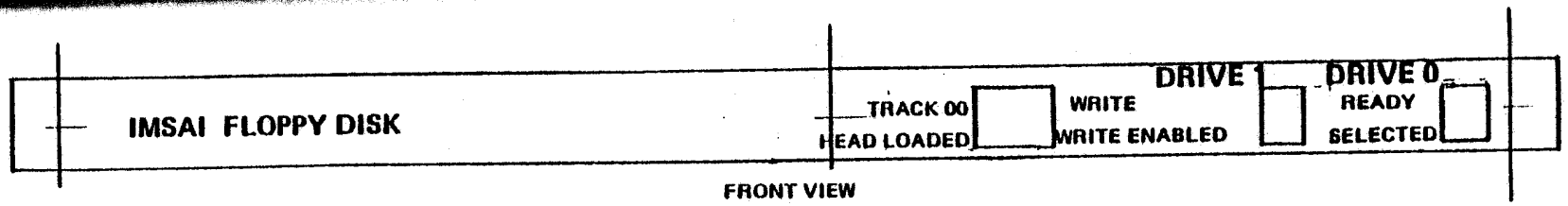
BACK SIDE (CIRCUIT SIDE)



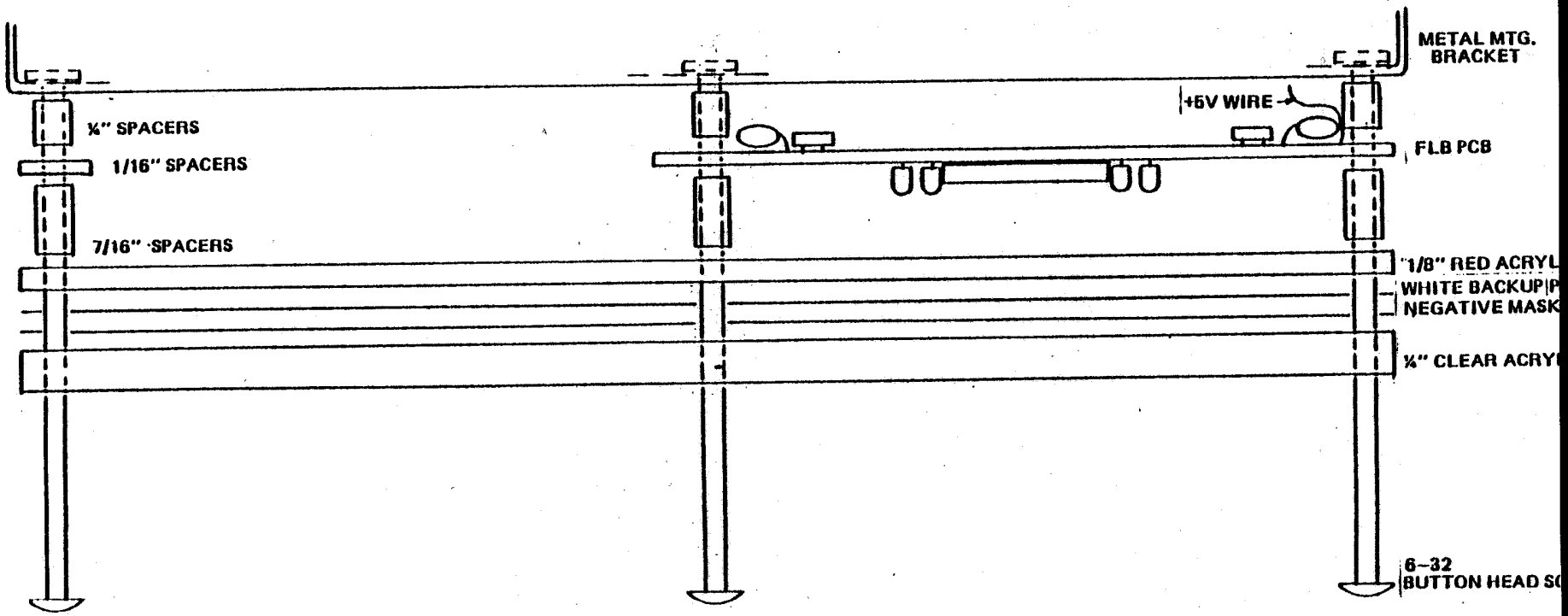
* Make sure the disk capacitor does not interfere with the mounting spacer.

ASSEMBLY DIAGRAM

FLB REV. 0 3/76

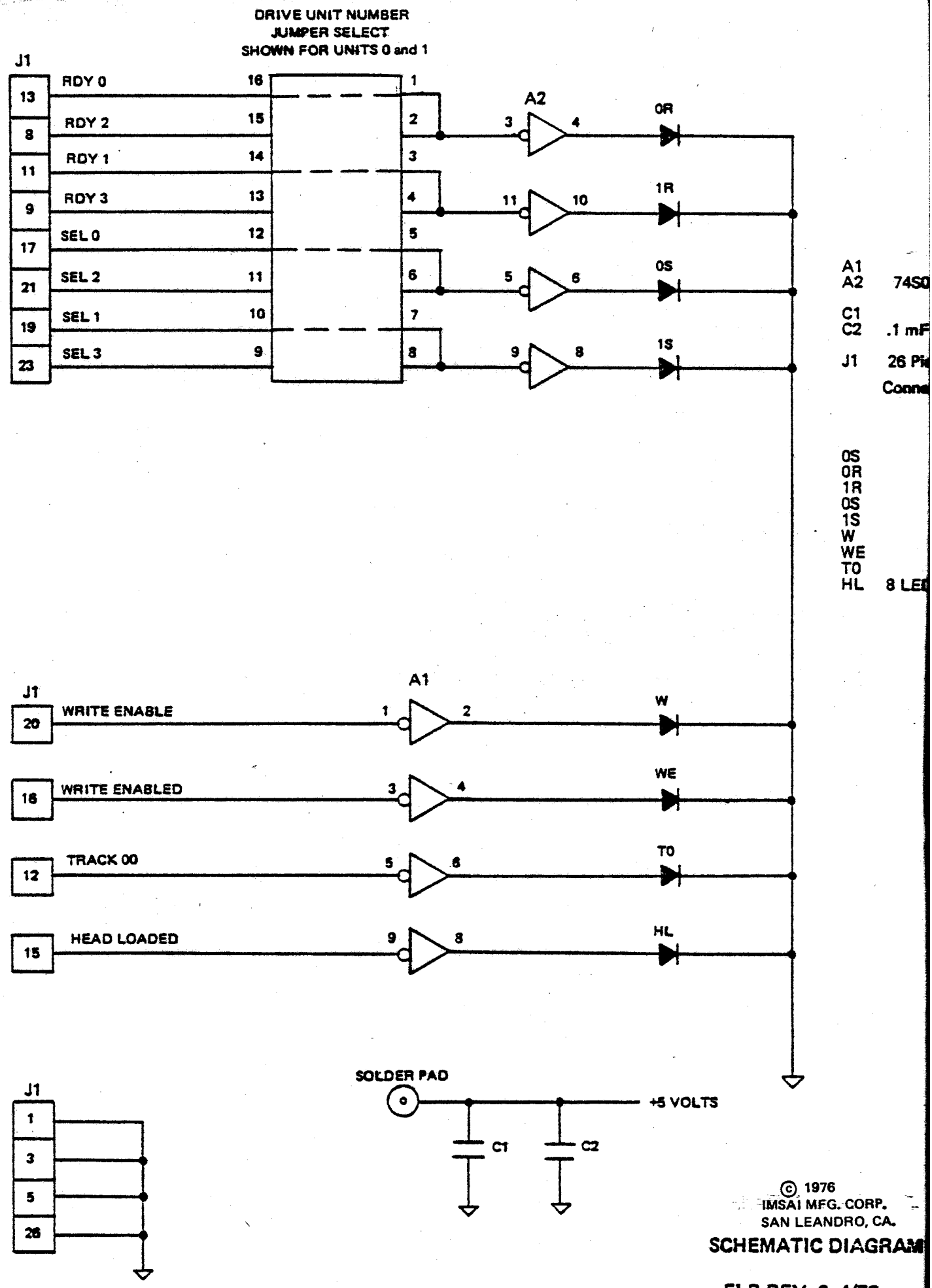


FRONT VIEW



TOP VIEW

ASSEMBLY DIAGRAM
FLB REV. 0 3/76


DRIVE UNIT NUMBER
JUMPER SELECT
SHOWN FOR UNITS 0 and 1
J1
13
RDY 0
8
RDY 2
11
RDY 1
9
RDY 3
17
SEL 0
21
SEL 2
19
SEL 1
23
SEL 3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
A2
3
4
11
10
5
6
9
8
0R
1R
0S
1S
A1
A2 74S0
C1
C2 .1 mF
J1 26 Pi
Conn
0S
0R
1R
0S
1S
W
WE
T0
HL 8 LE
J1
20
WRITE ENABLE
16
WRITE ENABLED
12
TRACK 00
15
HEAD LOADED
A1
1
2
3
4
5
6
9
8
W
WE
T0
HL
J1
1
3
5
26
SOLDER PAD
+5 VOLTS
C1
C2
© 1976
IMSAI MFG. CORP.
SAN LEANDRO, CA.
SCHEMATIC DIAGRAM
FLB REV. 0 4/76

BOARD: FLB

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
Solder	15-0000001	5'	
Connector	23-0400012	1	26 Pin Connector, SF 3429-1002
Capacitor	32-2010010	2	.1uF Disk Ceramic Capacitor
LED	35-3000001	8	Red LED
74S04	36-0740403	2	Hex Inverter
Cable	91-0400019	1	Cable Q Assembly
PC Board	92-0000008	1	FLB

ASSEMBLY INSTRUCTIONS

Following the Assembly Diagram in this section, mount the components on the board being careful not to form any solder bridges. The LED's should be mounted one at a time and pushed completely up against the board. The flat on each LED must be positioned toward the bottom of the board (away from the edge with the notch on it). Some of the LED leads cut off after soldering can be used to make the jumpers for the jumper select sockets. After making two bends in these leads so that they resemble a staple, insert them in the proper locations according to the diagrams in the User Guide and solder them in place, clipping any excess on the back of the board.

The connector can then be inserted into the hole pattern from the component side of the board and held firmly against the board while two diagonally opposite pins are soldered on the reverse side. Then, solder the rest of the pins. NOTE: the rest of the components are mounted on the reverse side of the board (the reverse side of the board is the side with no labelling except pin numbers on the connector).

Mount the two 74S04's in the two 14-pin IC patterns taking care that pin 1 is toward the end of the pattern with the diamond pointed pad (pin 1 toward the top of the board with the notch). Solder these in place taking care not to form any solder bridges where traces run between pins. Soldering these pins is done from the component side of the board.

Mount the two .1uF capacitors in the holes provided next to the 74S04's bending them over so that they lay flat against the board. Take care that any insulation extending down the length of the lead is cracked off so that when the lead enters the hole it is bare. Also, take care that the .1uF capacitor near the left end of the board is mounted close enough to the holes that the capacitor body does not interfere with the ¼" spacer on the mounting screw. The two capacitors should be soldered in place and the leads clipped off.

Cut the stranded wire into one 12 inch and one 6 inch length and strip each end about 3/16". Connect the 6" length to the female connector pin and the 12" to the male connector pin. If the proper crimping tool is not available, the crimping tabs can be folded over with a pair of pliers, first one and then the other over the top of the first and the wire soldered. The two pins should

then be inserted into the plastic bodies pushing them in from the rear until they click into place. Put the male pin in the body piece with the larger diameter section near the front. Put the female pin in the plastic body piece which is a small diameter for the full length. The front of this piece is the end with the two small tabs which lock it into the mating body piece.

The pin should be inserted from the other end from these tabs. Take the free end of the 12" wire and insert and solder it in the hole marked +5 on the upper right-hand corner of the FLB. Take the other end of the 6" piece and solder it into the pad on the +5 volt line on the back of the FPS. This soldering pad is located between the two heat sink areas, adjacent to R39 (.47 Ohm), and is connected to the +5 volt regulator terminal. This wire should be inserted from the component side of the FPS and soldered from the rear side so that the wire does not have to go around the edge of the FPS on its way to the FLB board.

The board is now ready to mount, with the acrylic front panel, to the metal mounting bracket (piece D). Take the negative front panel mask and using either scissors or a sharp knife and a straight edge, trim the negative mask to the inside of the clear cut-lines. Do the same with the printed white back-up sheet. On the back-up sheet also cut out the three black areas to enable the indicator lights to be seen. The three black areas are already printed slightly oversize of the windows in the negative mask so that you should cut right on the edge of the black rather than somewhere outside of it. If the holes are cut too wide, you may extend into the area of the legends.

Should all or part of any of the letters be dark after assembly, check to make sure that the letters have the white back-up fully behind them.

When the masks are cut out, you are ready to assemble the plastic panel. Take care to keep all the pieces extremely clean during these steps so that the finished panel will not have specks of dust trapped between. Should some dust get on any of the pieces, it may be wiped off with a very slightly damp lintless rag. If the rag is dampened with alcohol, it will help remove any finger prints as well.

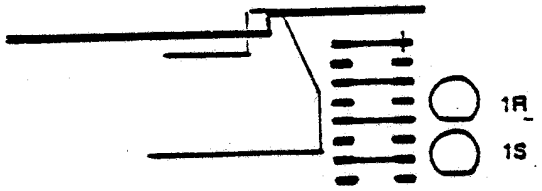
Examine the clear and red plastic pieces (wrapped in protective paper) to determine which are the right and left ends and top and bottom. Note that the spacing between the center and right screw is less than the space between the center and left screw. Also note that the spacing between the screws and the bottom is less than between the screws and the top.

Remove the protective paper from the clear piece and lay it front down on the table. Carefully lay the negative mask and white back-up sheet on the plastic. Next, remove the protective paper from the red piece and place it over the others. Lift the assembly and push the three black button head screws through the three holes and set the entire unit face down. Slide the three 7/16" plastic spacers on the three black screws then place the FLB on the two right hand screws with the indicators facing the panel. Place the 1/16" washer on the left hand screw and slide the three ¼" spacers, one each, onto the screws and rotate the whole assembly backwards so that the panel is upright and neither the screws nor spacers can drop off.

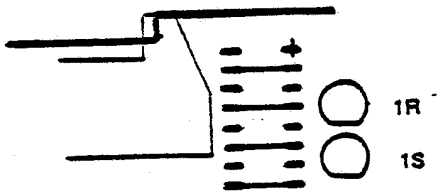
Screw the assembly onto the metal mounting rail (piece D) first starting all three screws and tightening. The front panel assembly is now ready for mounting in the cabinet.

JUMPER SELECT FLB

JUMPERS FOR DRIVES 0 and 1



JUMPERS FOR DRIVES 2 and 3



USER GUIDE

Follow the example shown to jumper the jumper select socket so that the READY and SELECT lines will respond to the proper drives. Note that if frequent changes are expected, the jumper socket is arranged such that a dip switch may be installed to make frequent changes more convenient. The only further consideration in using this board is to plug in the +5 volt power and signal cable and mount above the drives in the cabinet.

FLOPPY DISK SYSTEM

FLOPPY DISK CABINET

14860 Wicks Boulevard
San Leandro, California 94577

FUNCTIONAL DESCRIPTION----------

The Floppy Disk Cabinet houses up to two CalComp Model 140 Floppy Disk Drives. It is designed to use the IMSAI FLB Light Display Board, and the IMSAI FPS Power Supply Assemblies.

The cabinet is available with a Table Top Cover or with Rack Mount Hardware.

DIMENSIONS: The outside dimensions of the Table Top Model are 7" x 17" wide x 20" deep. The Drive Door handles extend 0.95" beyond the front plane of the cabinet.

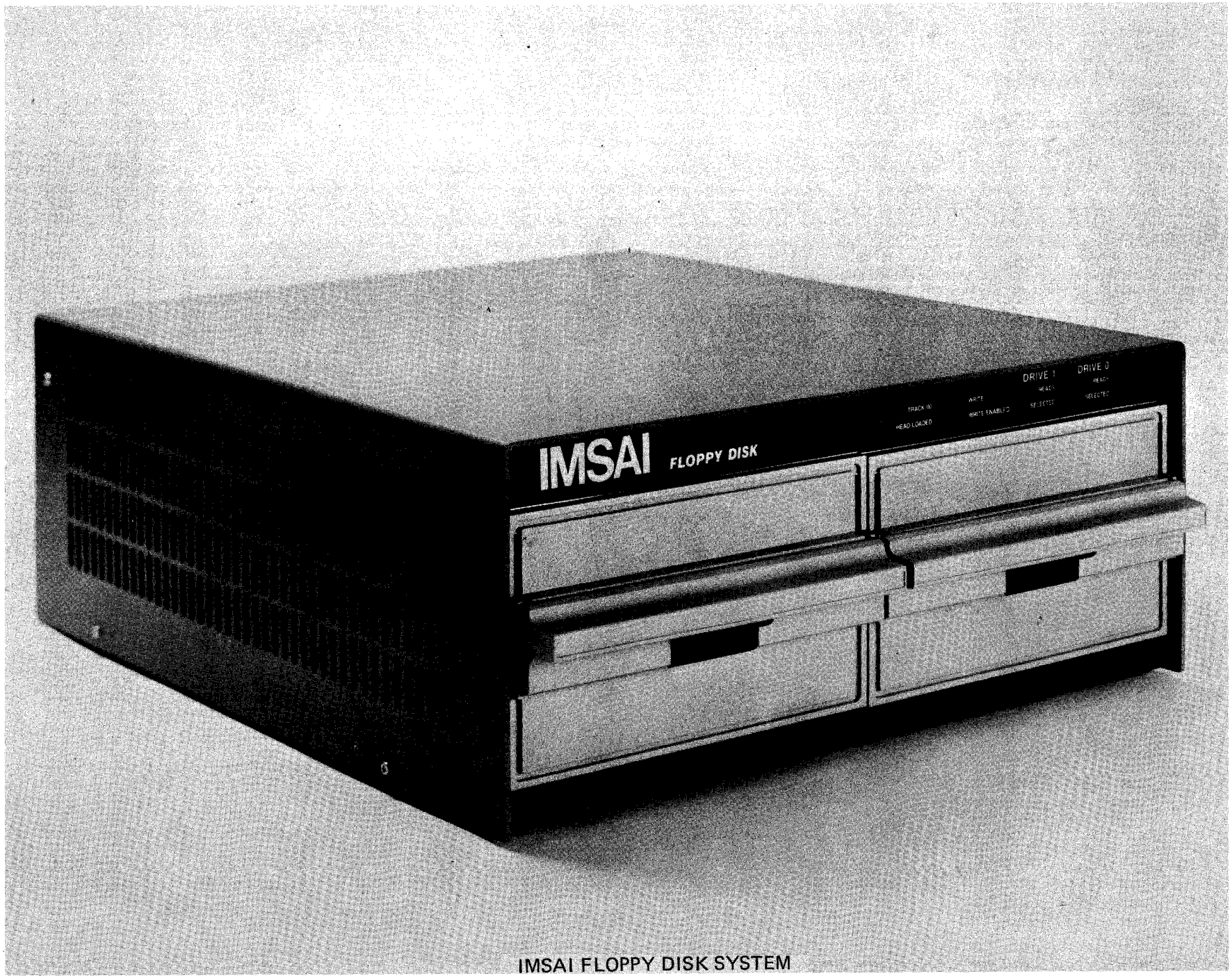
The Rack Mount Version provides for standard ear mounting in a 19" rack. It uses an 8 3/4 " panel space.

APPEARANCE: Both the Table Top and Rack Mount Versions of the Floppy Cabinet are designed to match the respective versions of the IMSAI 8080 cabinets.

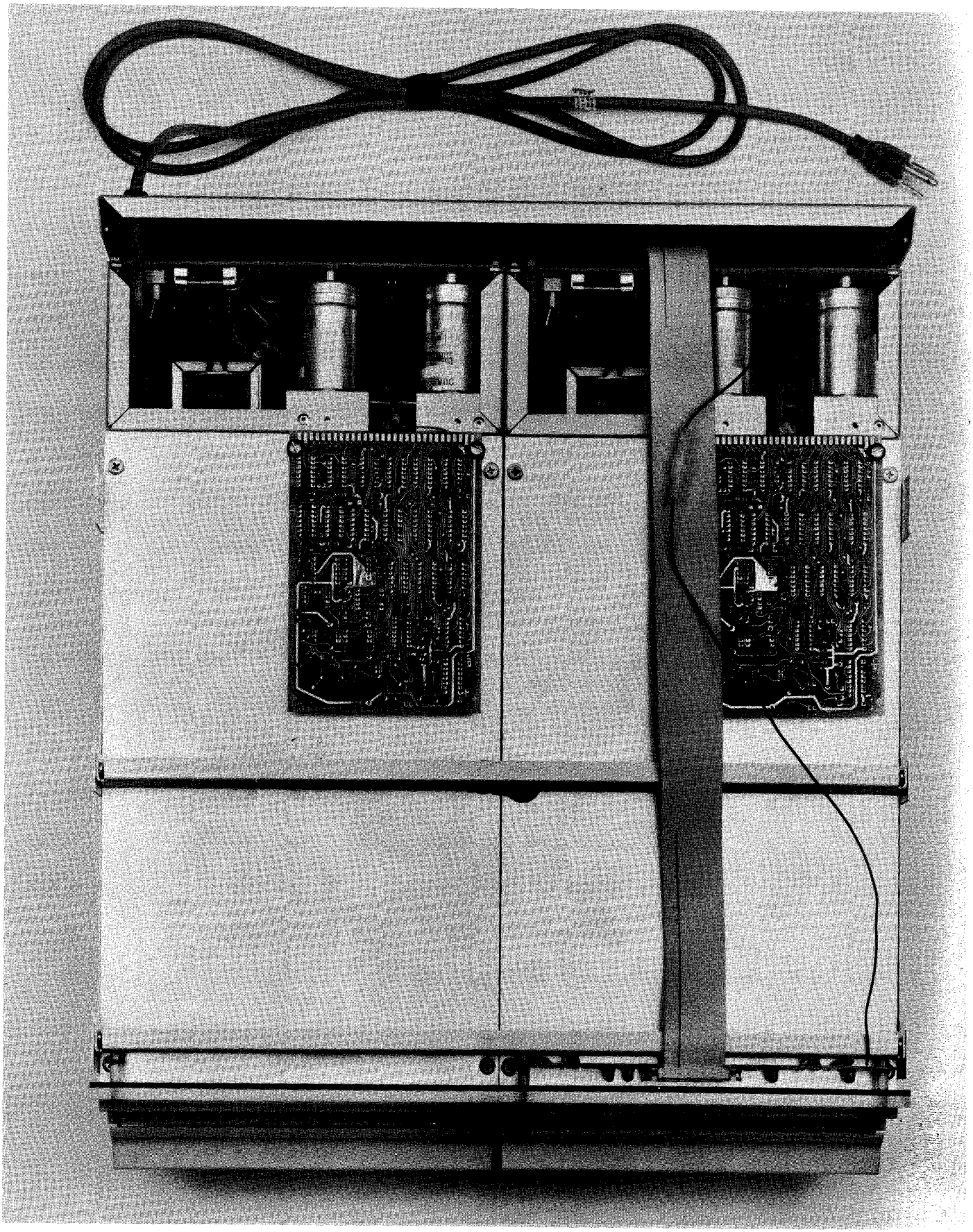
POWER AND COOLING: An AC power switch is provided to serve as the power on/off switch for up to two drives.

Cooling is accomplished through the use of an inboard fan and cooling vents in the chassis. The cooling system is designed to support the positive pressurization system used in the Model 140 Drive.

EXTERNAL CONNECTIONS: The back panel has provision for mounting two 25 pin D Type connectors to accomodate a four drive daisy chain system.



IMSAI FLOPPY DISK SYSTEM



IMSAI FLOPPY DISK SYSTEM (without Blue Cover)

FDS CHASSIS
Parts List

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
Screw	20-3702001	4	6-32x3/4" Phillips Pan Head Machine
Screw	20-3302001	20	6-32x5/16" Phillips Pan Head Machine
Screw	20-4506001	8	8-32x3/8" Phillips Flat Head 100% Machine
Screw	20-3406001	8	6-32x3/8" Phillips Flat Head 100% Machine
Nut	21-3120001	4	6-32 Hex Nut
Lockwasher	21-3350001	4	#6 Internal Star Lockwasher
Connector	23-1700003	1	Molex Receptacle, 03-09-1031
Bushing	24-0600001	1	Strain Relief Bushing
Hole Plug	24-0700001	1	½", Smith 3092 Nylon or 653 Metal
Feet	28-0400001	6	Rubber Feet
Foam Tape	28-0600001	2"	Foam Tape, ½"x½" Thick, Adhesive-Backed, 2 Sides
Foam Tape	28-0600002	17"	Foam Tape, 5/8"x5/8", Black Closed-cell Neoprene Sponge, 100% F, Boyd Industrial Rubber Co. SC-41
Fan	34-0100001	1	
Fan Guard	34-0200001	1	
Cable	91-0400024	1	Cable AB Assembly
Cable	91-0400025	1	Cable AC Assembly
Cable	91-0400026	1	Cable AD Assembly
	93-4020001	2	Floppy Disk System Side Plates, Rev. B
	93-4020002	1	Floppy Disk System Base Stiffener, Rev. B
	93-4020003	1	Floppy Disk System Center Brace
	93-4020004	1	Floppy Disk System Front Brace

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
	93-4020005	1	Floppy Disk System Painted Front Rail, Rev. B
	93-4020006	1	Floppy Disk System Back Panel, Rev. B
	93-4020007	1	Floppy Disk System Base Plate, Rev. B

ASSEMBLY INSTRUCTIONS----------

( ) 0.

Unpack and check all parts against the parts list enclosed with the package.

BACK PANEL ASSEMBLY

( ) 1.

Insert one end of the AC Power Cord (CABLE AC) through the 1/2" hole in the upper left corner of the back panel (viewed from the rear). Verify that the end of CABLE AC with the three Molex pins is on the inside. Pull approximately 6" of cable through the hole and secure in place with one grommet.

( ) 2.

Assemble the 3 pin Molex socket on the end of CABLE AC as follows. Insert the BLACK wire into the top (pointed end) of the connector body from the rear of the connector. Push until the pin snaps into place.

Insert the GREEN WIRE into the center position of the connector body from the rear of the connector. Push until the pin snaps into place.

Insert the WHITE WIRE into the bottom (square edge) of the connector body from the rear of the connector. Push until the pin snaps into place.

( ) 3.

Insert the Power Switch into the 1/4" hole in the back panel and fasten with the hardware provided. Note that the Power Switch is connected to CABLE AB and terminates in a Male 2-pin Molex connector.

( ) 4.

Mount the fan on the inside of the back panel and the fan guard on the outside of the back panel using four #6 screws, nuts and lockwashers. Verify that the fan is installed with the arrow (Air Flow) pointing OUT of the cabinet and that the fan power connections are toward the right as you face the rear of the back panel.

CHASSIS ASSEMBLY

( ) 5.

Mount the bottom cross brace to the base plate using six #6-32 screws.

( ) 6.

Mount the two side pieces to the baseplate using four #6-32 screws. Orient the side pieces so that their outside faces align with the outside edges of the base plate.

( ) 7.

Attach the six rubber feet to the bottom of the base plate. Peel off the protective backing and position the feet equidistant along the right and left edges of the base plate bottom approximately 1" from the edge.

( ) 8.

Draw a line across the width of the base plate, approximately 1/8" behind the line which intersects the rear edges of the two side pieces.

( ) 9.

If two drives are to be installed in this cabinet, mount the adhesive backed foam strip along the width of the base plate, directly behind the line drawn in step 8.

If one drive is to be installed in this cabinet, cut the adhesive backed foam strip to half the width of the base plate. Mount this strip along the right half of the base plate, directly behind the line drawn in STEP 8.

( ) 10.

Place one drive into the right side of the cabinet and fasten it to the right side piece with four #8-32 flat head screws.

If a second drive is to be used, mount it, as above, on the left side of the cabinet, and fasten it to the left side piece with four #8-32 flat head screws.

( ) 11.

If only one drive is to be installed, mount the grey filler panel in the space normally occupied by the face of the second drive. Fasten it to the first drive and to the left side piece with four #8-32 flathead screws.

Then mount the rear filler piece in the space normally occupied by the rear of the second drive. Attach it to the base plate with one #6-32 pan head screw. Fasten it to the first drive with one #8-32 flathead screw, and to the left side piece with one #6-32 phillips head flathead screw (TOP) and one #8-32 flathead screw (BOTTOM).

( ) 12.

Place the center upper cross piece between the two center tabs of the side pieces, with the flat side facing the front of the cabinet. Insert a foam pad between the cross piece and the center of each floppy drive, and fasten the cross piece to the side pieces with four #6-32 flathead screws. Use enough foam so that a reasonable amount of downward pressure is required to mount the cross piece.

( ) 13.

Mount the grey filler rail beneath the front of the floppy drives. Fasten it to the front of the base plate with four #6-32 pan head screws.

( ) 14.

Place the front cross piece and FLB Assembly between the two front tabs of the side piece. Fasten in place with four #6-32 flat head screws.

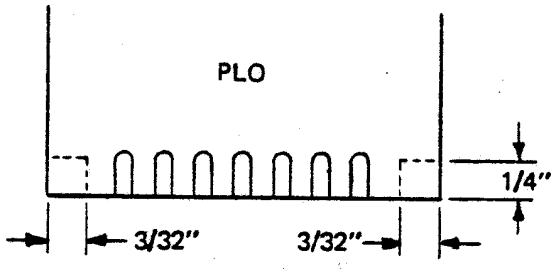
( ) 15.

Mount the two card guides at the right rear of the cabinet. Fasten each card guide with two #4 screws, positioning the lockwashers between the baseplate and the bottom of the card guide. Verify that the slots in the card guides face each other.

( ) 16.

Modify the PLO Board as follows: Snap off the two white nylon posts at the TOP of the card (opposite the connector end of the card).

Using a nibbling tool, cut away the two bottom corners of the card adjacent to the first and last connector contacts. Cut 1/4" up from the bottom edge, parallel to the connector contacts and cut 3/32" in from the side edge of the board. You will be left with a rectangular cutout on the right and left bottom corners with dimensions 1/4" deep x 3/32" wide.



INTERNAL CABLING

( ) 17.

Identify the two CABLE E's in a Dual Drive Kit or the one CABLE E in a Single Drive Kit. CABLE E may be identified by the 25 pin D Type connector on one end, and 26 pin connector in the middle and on the opposite end of the cable.

NOTE: In a Dual Drive Kit, one CABLE E is longer than the other.

( ) 18.

Mount the 25 pin D Type Connector of CABLE E, (the long CABLE E for a Dual Drive Kit), in the leftmost connector opening in the back panel (viewed from the rear). Verify that the cable extends down towards the bottom of the back panel and fasten with the cable hardware provided.

If this is a Dual Drive Kit, mount the second CABLE E in the remaining connector opening on the right hand side of the back panel (viewed from the rear). Verify that the cable extends down towards the bottom of the back panel and fastens with the cable hardware provided.

( ) 19.

Position the backpanel next to the rear of the cabinet in its proper mounting position. Connect the CABLE E on the left (viewed from the rear) to the Drive on the left and to the FLB as follows.

From the D Type connector make a 180 degree fold just before the middle 26 pin connector. Attach this connector to J2 (LEFT) of the FPS. Attach the remaining end connector to the FLB board by bringing the cable up over the top surfaces of the Drive.

For a Dual Drive Kit, attach the remaining CABLE E between the two drives as follows. From the D Type connector make a 180 degree fold just before the middle 26 pin connector. Attach this connector to J3 (RIGHT) on the FPS of the second drive. Bring the cable out towards the rear and make a 90 degree fold to the left. At the point where the cable passes in front of J3 (RIGHT) on the FPS of the first drive make a 90 degree fold towards the rear of the cabinet. Then make a 180 degree fold so that the cable now extends towards J3 on the FPS of the first drive. Make another 180 degree fold just before the last 26 pin connector and insert it into J3 on the FPS of the first drive.

( ) 20.

Plug the AC power connector (CABLE AC) into the AC input connector (CABLE V at J5) on the FPS of the first drive.

If this is a Dual Drive Kit, plug the CABLE X from the FPS of the first drive (coming from the board location AC CONT) into the AC input connector (CABLE V at J5) on the FPS of the second drive.

( ) 21.

Connect CABLE AB from the power switch to the CABLE AB from the FPS of the first drive.

( ) 22. Connect one end of CABLE AD to the fan power terminals and connect the other end to the remaining CABLE X on the FPS (from area AC CONT). This will be on the FPS of the second drive in a Dual Drive Kit.

( ) 23. Connect one end of CABLE AA to the 8 pin connector at J4 on the FPS of the first drive. Note that the empty position in the 8-pin connector of cable AA is pin 8 and should go to the pin of J4 farthest from the center of the card. Connect the remaining end to the PLO card, with the lettered side of the connector on the component side of the PLO Board.

( ) 24. Position the back panel and fasten into place with four #6-32 screws.

TABLE TOP COVER INSTALLATION

( ) 25. After testing, position the Tabletop cover and fasten into place with six #6-32 screws. Assembly is now complete.

RACK MOUNT INSTALLATION

( ) 26.

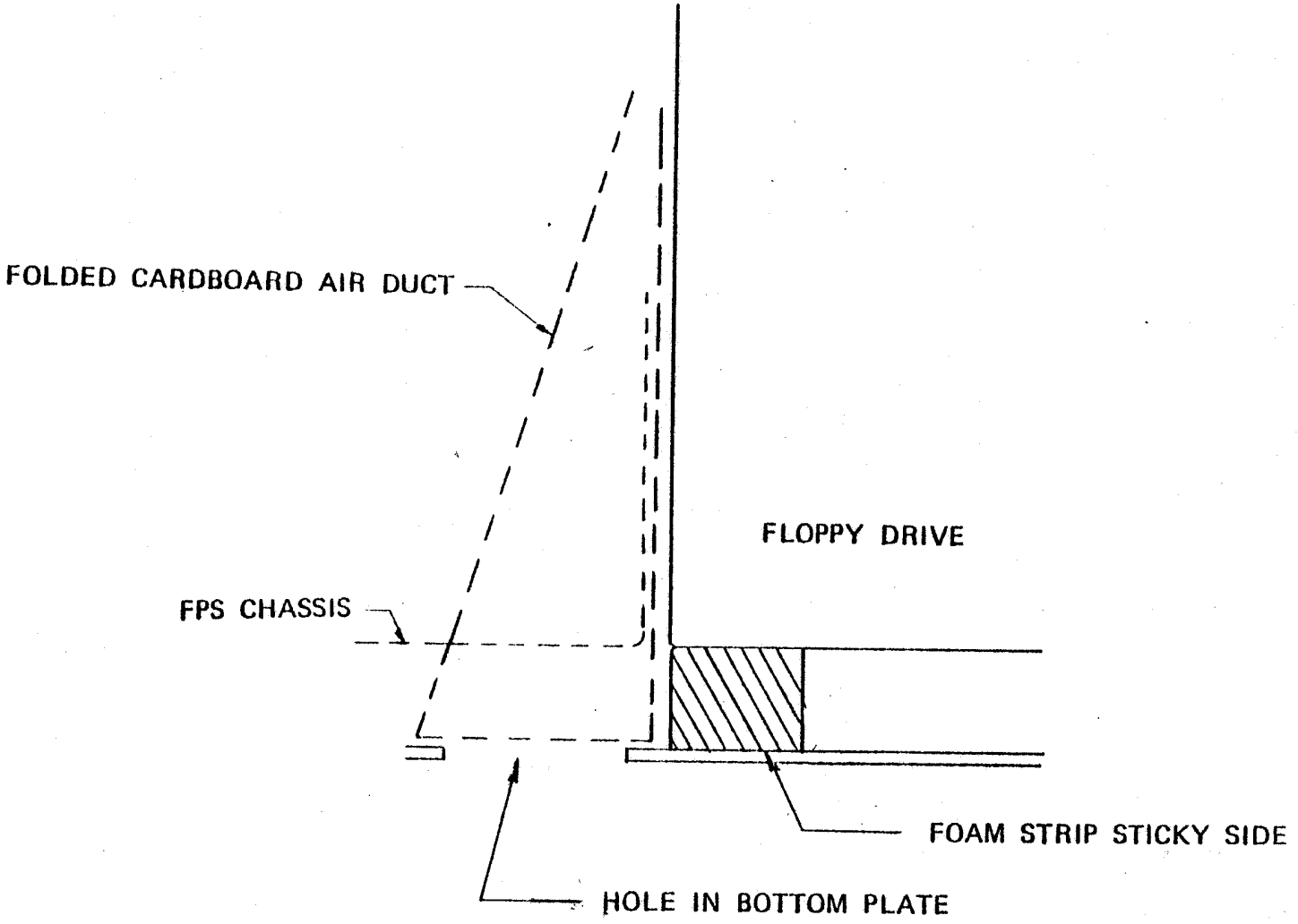
After testing, position the two side rails so that the front panel will line up with the front surface of the side pieces. Fasten each rail to the chassis with three #6-32 screws.

( ) 27.

Mount the unit in the rack using standard flat head screws on the front ears. It is desireable to secure the rear of the side rails to a point in the back of the rack.

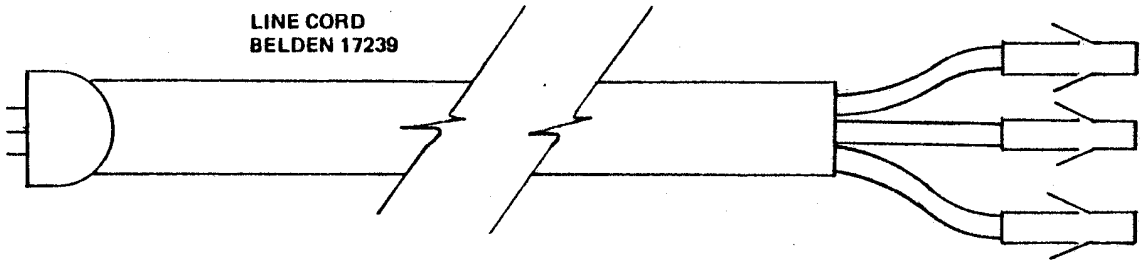
( ) 28.

Install the grey bezel and fasten it to the rack using four screws. Assembly is now complete.



CROSS-SECTION VIEW OF CARDBOARD DUCT IN PLACE

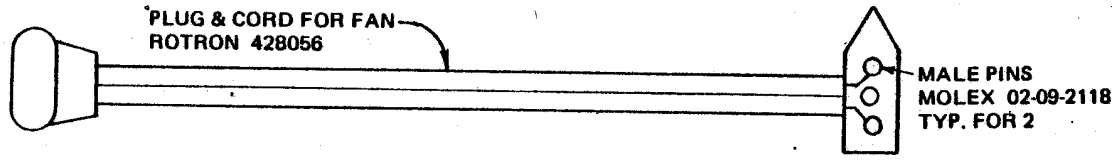
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL	2/77	PRU



TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		IMSAI MFG. CORP. SAN LEANDRO, CA.		
APPROVALS	DATE	FLOPPY DISK SYSTEM CABLE AC ASSEMBLY 91-0400025		
DRAWN PRU	2/1/77			
CHECKED D. Carroll	2/2/77	SCALE	SIZE	DRAWING NO. 91-1040025
		DO NOT SCALE DRAWING		SHEET

BISHOP GRAPHICS, INC.
REORDER NO. 20620

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL	2/1/77	PRU



TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS ± DEC ± ANGLES ±		IMSAI MFG. CORP. SAN LEANDRO, CA.		
APPROVALS	DATE	FLOPPY DISK SYSTEM CABLE AD ASSEMBLY 91–0400026		
DRAWN PRU	2/77			
CHECKED D. Carroll	2/2/77	SCALE	SIZE	DRAWING NO. 91-1040026
		DO NOT SCALE DRAWING		SHEET

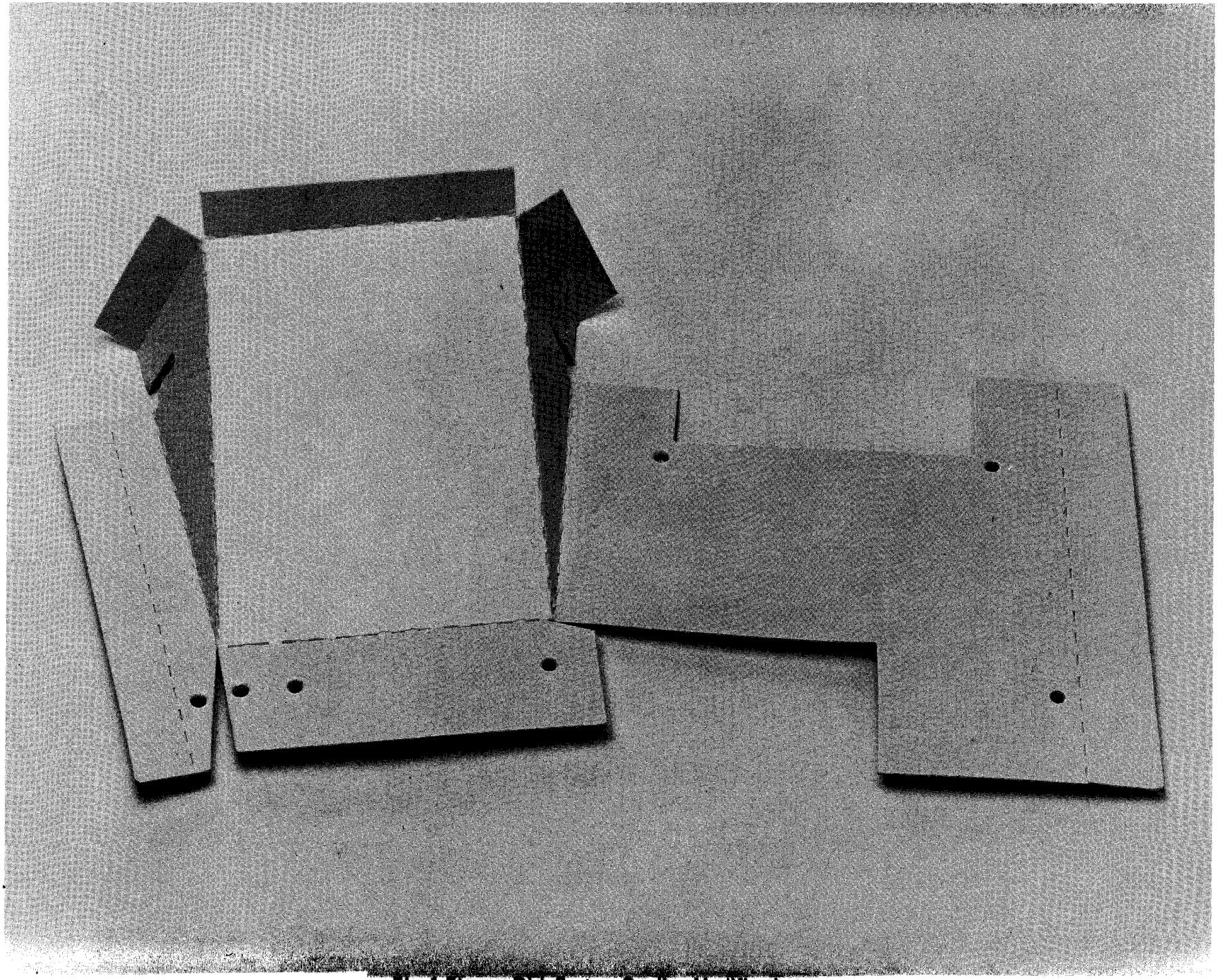


Fig. 1 Floppy Disk System Cooling Modification

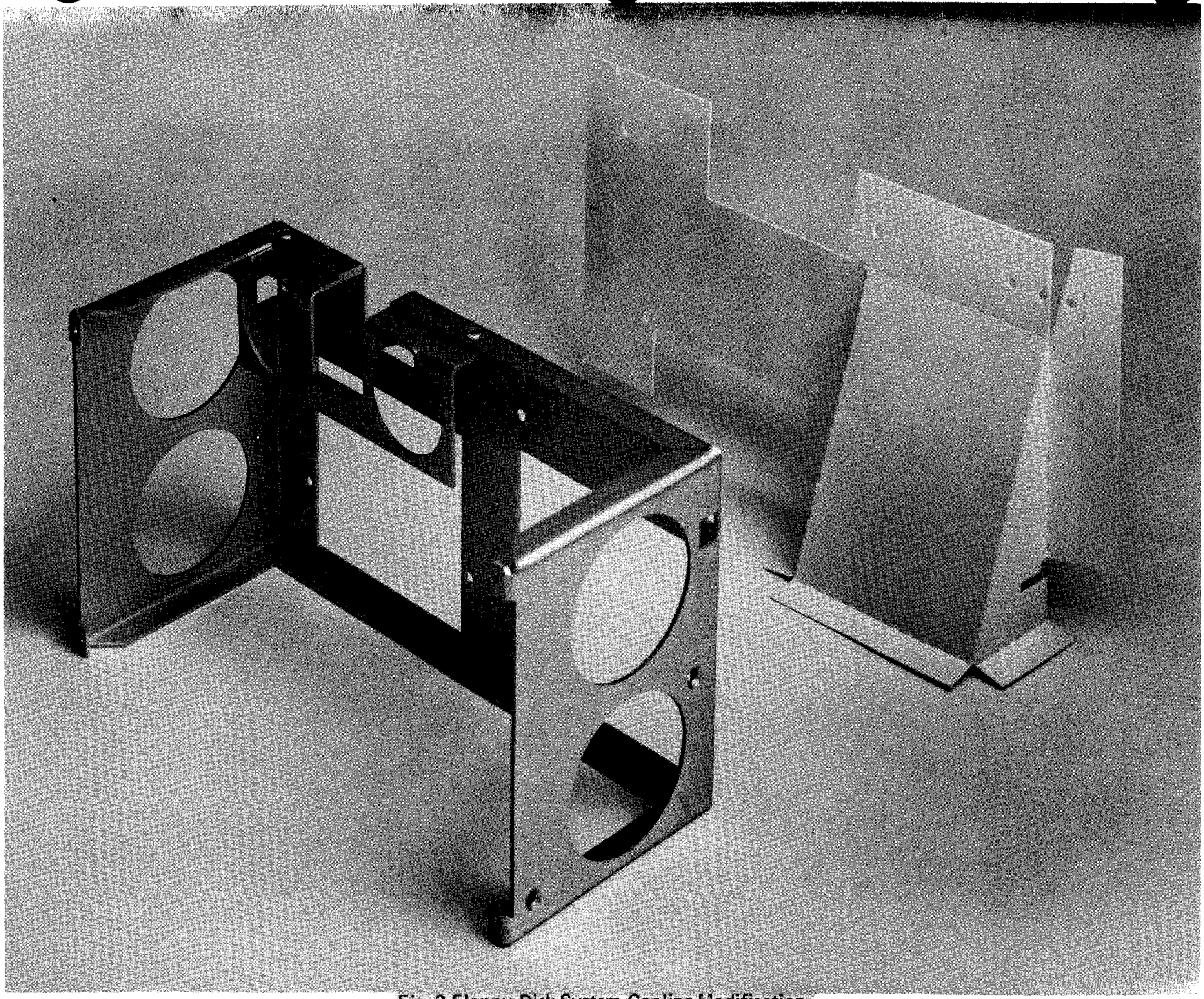


Fig. 2 Floppy Disk System Cooling Modification

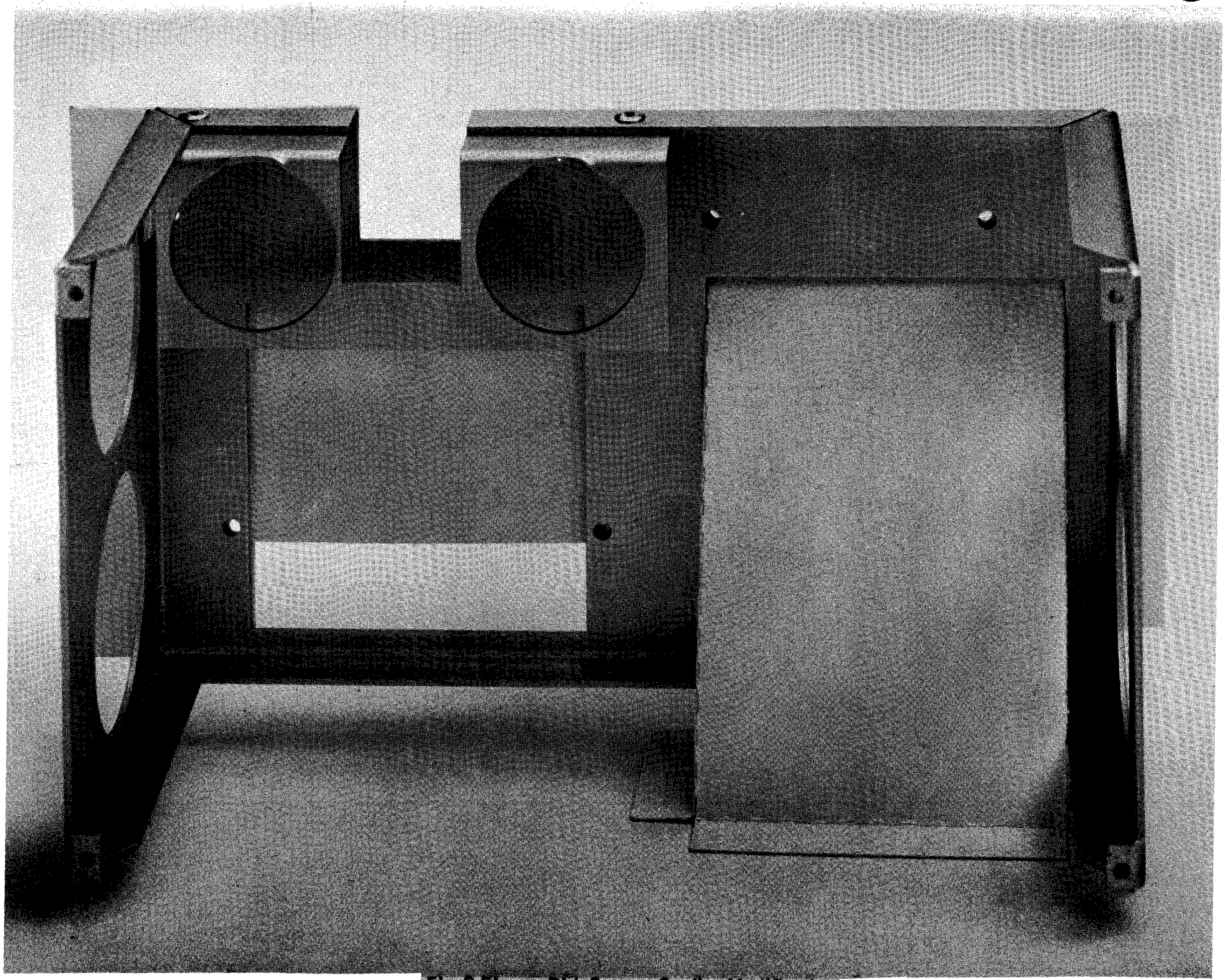
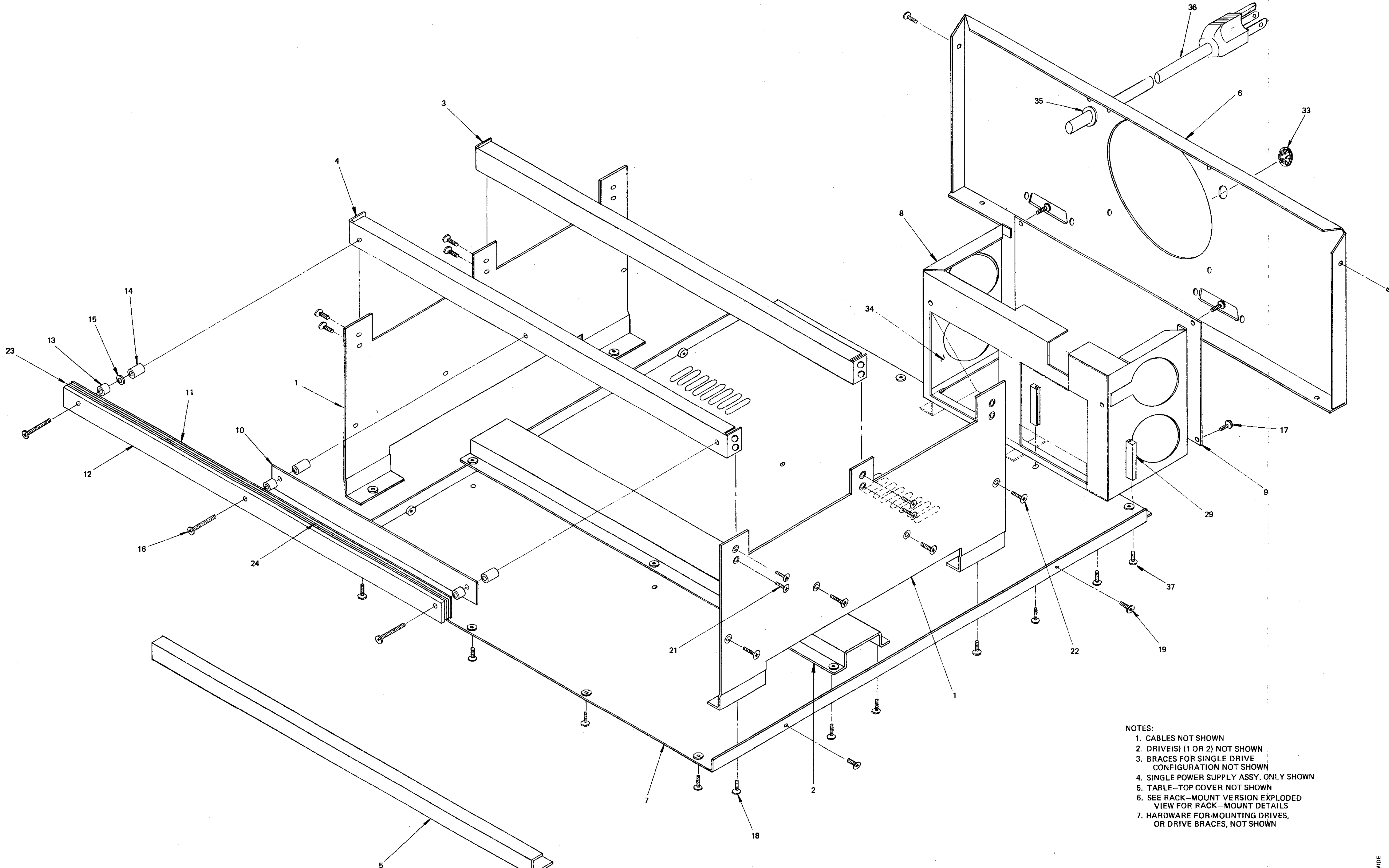


Fig. 3 Floppy Disk System Cooling Modification

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ORIGINAL	3-14-77	C.O.L.

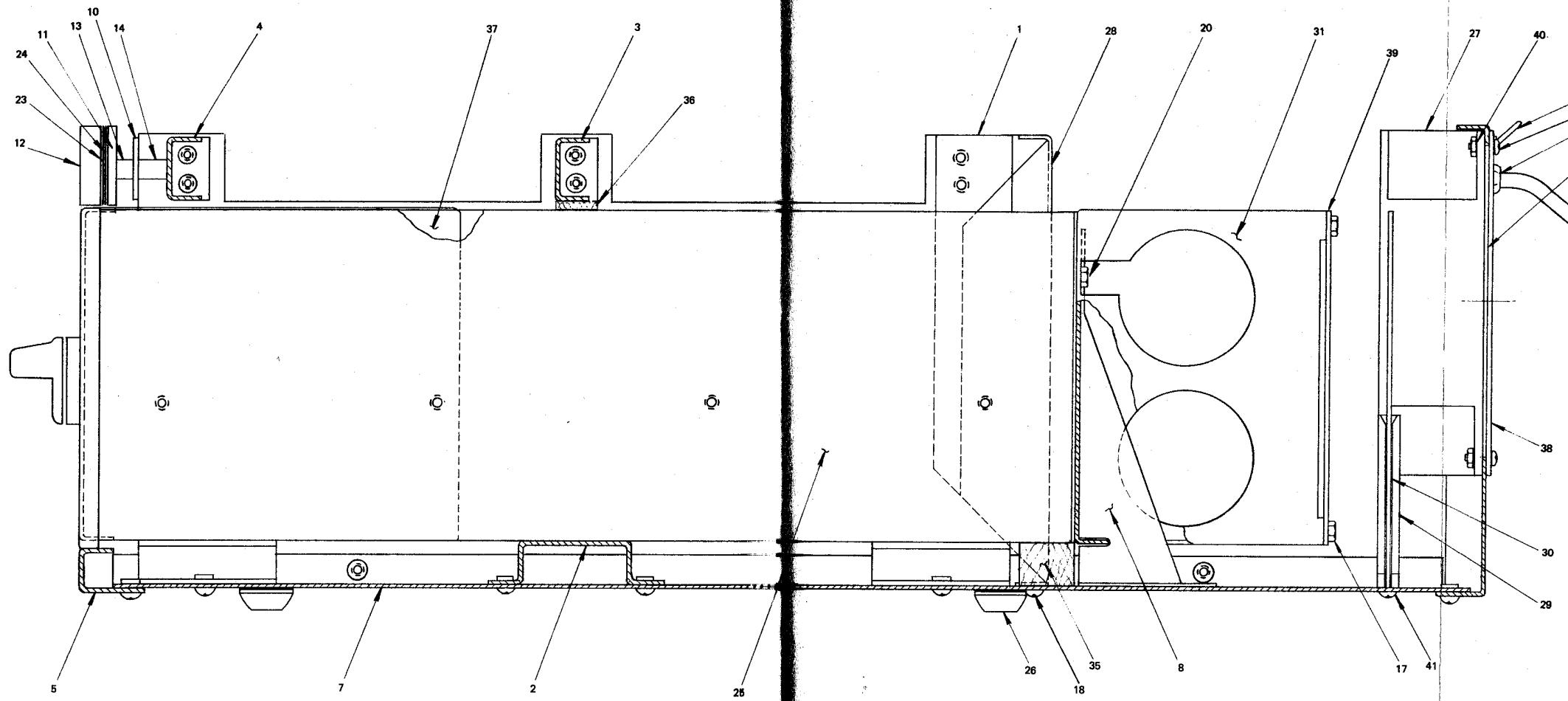


1 SIDE PLATE
2 STIFFENER
3 REAR BRACKET
4 FRONT BRACKET
5 PANEL FILLER
6 REAR PANEL
7 BASE PLATE
8 FLOPPY POWER SUPPLY CHASSIS (1 ONLY SHOWN)
9 FPS P.C.B. ASSY (1 ONLY SHOWN)
10 FLB P.C. B. ASSY
11 RED ACRYLIC PANEL
12 CLEAR ACRYLIC PANEL
13 SPACER 1/4" O.D. x 1/4" (QTY.3)
14 SPACER 1/4" O.D. x 7/16" (QTY. 3)
15 1/16" WASHER (QTY. 1)
16 SCREW 6-32 x 1½" ALLEN HEAD (QTY. 3)
17 SCREW 6 x 1/4" SELF-TAPPING (QTY.4)
18 SCREW 6-32 x 1/4" PAN HEAD (QTY. 18)
19 SCREW 6-32 x 1/2" PAN HEAD (QTY. 6) (MT. CVR. OR RACK MT.)
20 SCREW 8-32 x 1/4" PAN HEAD (QTY.2)
21 SCREW 6-32 x 3/8" 100° FLAT HEAD (QTY. 8)
22 SCREW 8-32 x 3/8" 100° FLAT HEAD (QTY. 8)
23 FILM MASK
24 WHITE PAPER MASK
25 C-140 DRIVE (QTY. 1 or 2) (NOT SHOWN)
26 ADHESIVE-BACKED RUBBER FEET (QTY. 6) (NOT SHOWN)
27 FAN (NOT SHOWN)
28 SINGLE-DRIVE BRACE (FOR SING. DRIVE SYSTEMS) (NOT SHOWN)
29 CARD GUIDE (QTY. 2)
30 PLO BOARD ASSY (NOT SHOWN)
31 FAN GUARD (NOT SHOWN)
32 FOAM TAPE (NOT SHOWN)
33 1/2" DIA. HOLE PLUG
34 PAPER DUCT (INDICATED)
35 GROMMET
36 LINE CORD
37 SCREW 4-40 x ¼" WITH NO. 4 LOCKW.

NOTES:
1. CABLES NOT SHOWN
2. DRIVE(S) (1 OR 2) NOT SHOWN
3. BRACES FOR SINGLE DRIVE CONFIGURATION NOT SHOWN
4. SINGLE POWER SUPPLY ASSY. ONLY SHOWN
5. TABLE–TOP COVER NOT SHOWN
6. SEE RACK–MOUNT VERSION EXPLODED VIEW FOR RACK–MOUNT DETAILS
7. HARDWARE FOR MOUNTING DRIVES, OR DRIVE BRACES, NOT SHOWN

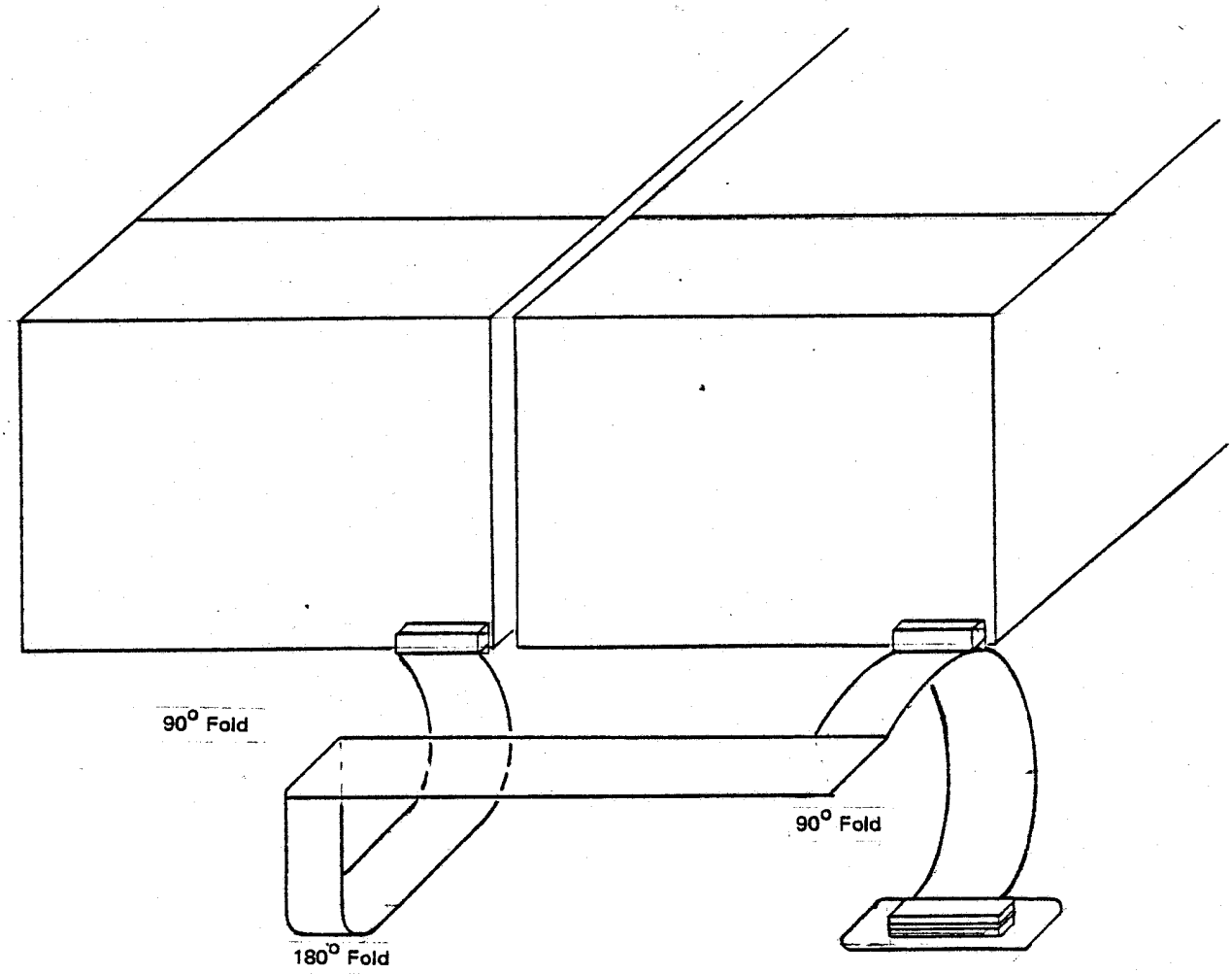
TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS ± DEC ± ANGLES ±		IMSAI MFG. CORP. SAN LEANDRO, CA.		
APPROVALS	DATE	FLOPPY DISK SYSTEM CHASSIS EXPLODED VIEW		
DRAWN C.O.L.	3/14/77			
CHECKED [signature]	3/17/77	SCALE —	SIZE D	DRAWING NO. 93-4020011
		DO NOT SCALE DRAWING		SHEET 1 OF 2

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ORIGINAL	3-14-77	G.D.L.



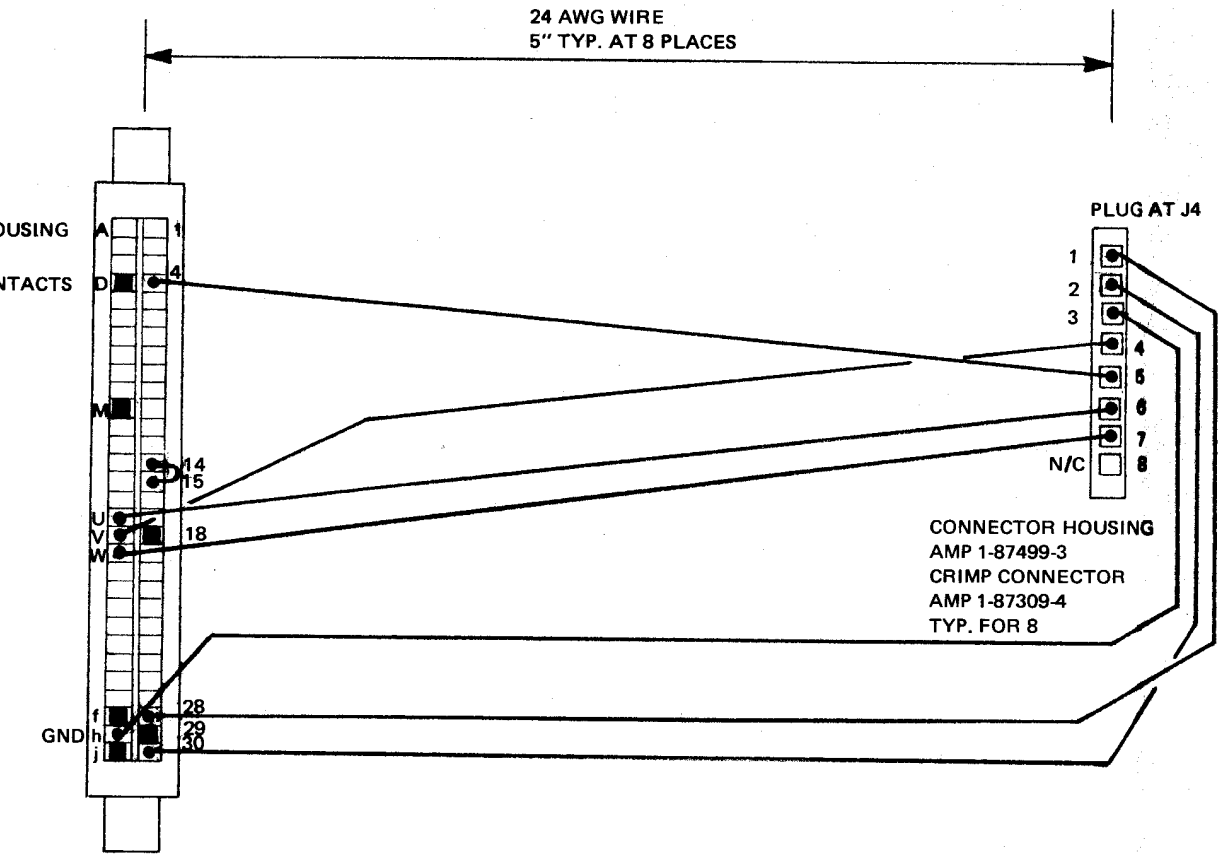
1 SIDE PLATE
2 STIFFENER
3 REAR BRACKET
4 FRONT BRACKET
5 PANEL FILLER
6 REAR PANEL
7 BASE PLATE
8 PAPER DUCT
9 FPS P.C.B. ASSY
10 FLB P.C.B. ASSY
11 RED ACRYLIC
12 CLEAR ACRYLIC
13 SPACER 1/4" O.D. x 1/4" (QTY. 3)
14 SPACER 1/4" O.D. x 7/16" (QTY. 3)
15 1/16" WASHER (QTY. 3)
16 SCREW 6-32 x 1¼" BUTTON HEAD (QTY. 3)
17 SCREW 6 x 1/4" SELF-TAPPING (QTY. 4)
18 SCREW 6-32 x 1/4" PAN HEAD (QTY. 18)
19 SCREW 6-32 x 1/2" PAN HEAD (QTY. 6)
20 SCREW 8-32 x 1/4" PAN HEAD (QTY. 2)
21 SCREW 6-32 x 3/8" 100° FLAT HEAD (QTY. 8)
22 SCREW 8-32 x 3/8" 100° FLAT HEAD (QTY. 8)
23 FILM MASK
24 WHITE PAPER MASK
25 C-140 DRIVE (QTY. 1 or 2)
26 ADHESIVE-BACKED RUBBER FEET (QTY. 4)
27 FAN
28 SINGLE-DRIVE BRACE (FOR SINGLE-DRIVE SYSTEM)
29 CARD GUIDE (QTY. 2)
30 PLO BOARD ASSY
31 FLOPPY POWER SUPPLY CHASSIS
32 LINE CORD
33 LINE CORD GROMMET
34 TOGGLE SWITCH
35 FOAM TAPE ¾" x ¾"
36 FOAM TAPE ¼" THICK
37 BLANK FRONT PLATE (SINGLE DRIVE SYSTEM)
38 FAN GUARD
39 FPS P.C. BOARD ASSY.
40 NUT 6-32
41 SCREW 4-40 x ¼" WITH NO. 4 LOCKW.

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		IMSAI MFG. CORP. SAN LEANDRO, CA.	
APPROVALS	DATE	FLOPPY DISK SYSTEM CHASSIS EXPLODED VIEW	
DRAWN G.D.L.	3-14-77		
CHECKED A. Rafla	3/17/77	SCALE —	SIZE D / DRAWING NO. 93-4020011
		DO NOT SCALE DRAWING	SHEET 2 OF 2



INSERT A
FOLDING THE INTER–DRIVE SIGNAL CABLE

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL	1/77	D. Carroll



NOTE:
Used on PLO Board Assembly

Use Crimp Tool AMP 90287-1.

Use Extraction Tool AMP 91073-1.

RETAINING SPRING
AMP 583691-2
TYP. FOR 3
CONTACTS
D
M
18

DUMMY CONTACTS
AMP 583857-6
TYP. FOR 3
CONTACTS
f
j
29

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC. ANGLES
± ± ±

APPROVALS	DATE
DRAWN PEU	1/10/77
CHECKED D. Carroll	2/2/77

FLOPPY SYSTEM
CABLE AA
ASSEMBLY
91-0400023

SCALE	SIZE	DRAWING NO.
—	B	91-2040023

DO NOT SCALE DRAWING | SHEET

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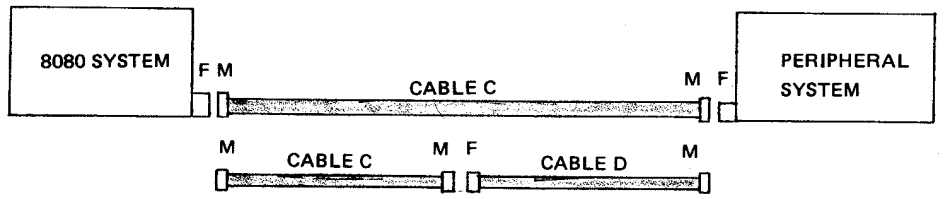
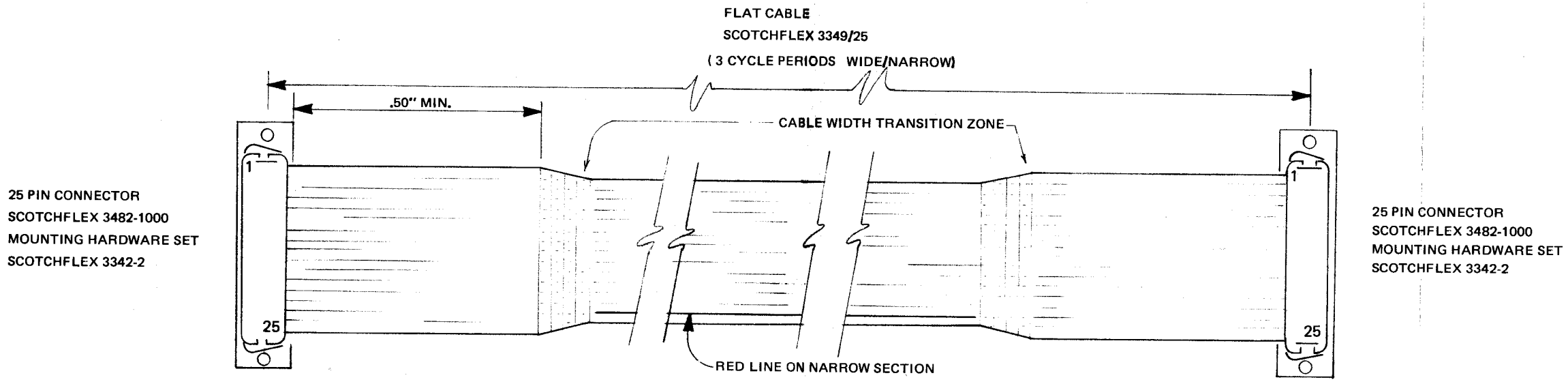


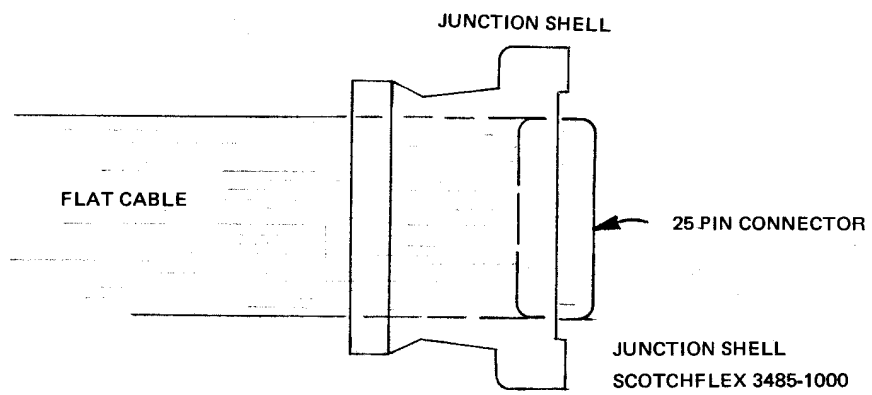
INTER CHASSIS CONNECTOR DETAIL

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL	8/76	
1	REVISED CABLE DIMENSIONS REVERSED SHELL	8/27/76	A. Holmes
2	MODIFIED TO SHOW INTER CHASSIS CONNECTOR DETAIL	10/25/76	D. Arnold

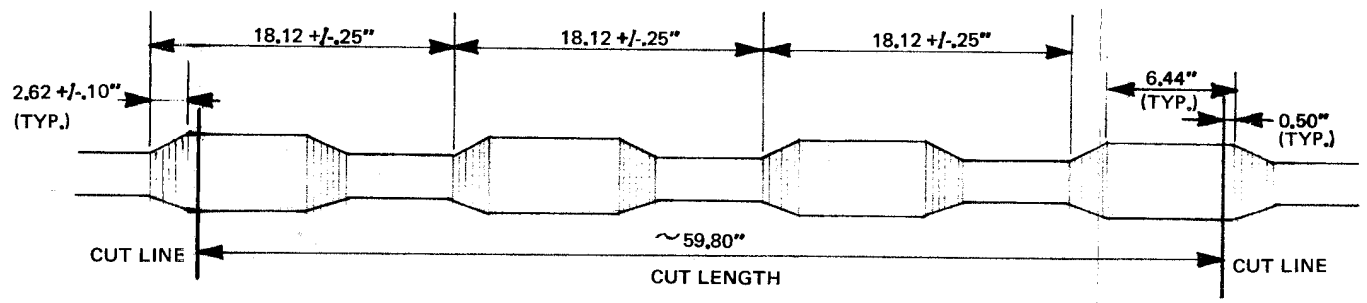


25 PIN CONNECTOR
SCOTCHFLEX 3482-1000
MOUNTING HARDWARE SET
SCOTCHFLEX 3342-2

25 PIN CONNECTOR
SCOTCHFLEX 3482-1000
MOUNTING HARDWARE SET
SCOTCHFLEX 3342-2



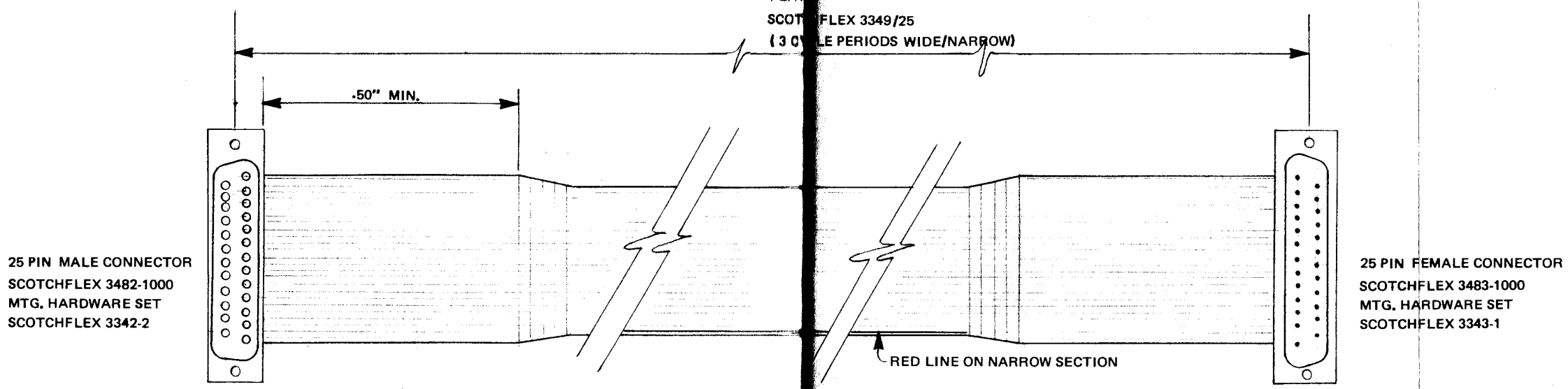
JUNCTION SHELL/ CONNECTOR DETAIL

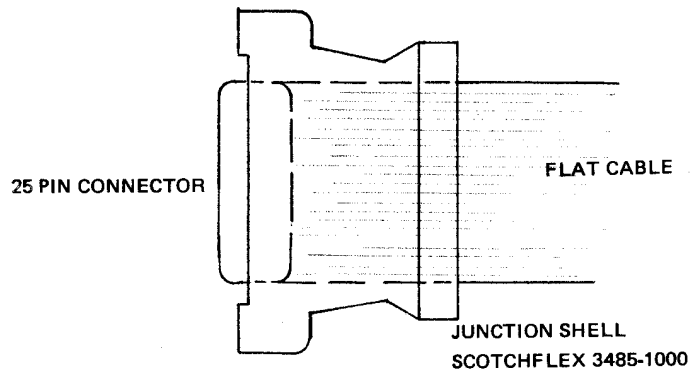


TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC. ANGLES ± ± ±		© 1976 IMSAI MFG. CORP. SAN LEANDRO, CA.		
APPROVALS	DATE	FLOPPY DISK SYSTEM CABLE C ASSEMBLY 91-0400004		
DRAWN YP	8/76			
CHECKED D. H.	9/11/76	SCALE	SIZE B	DRAWING NO. 91-2040004
		DO NOT SCALE DRAWING		SHEET 1 OF 1

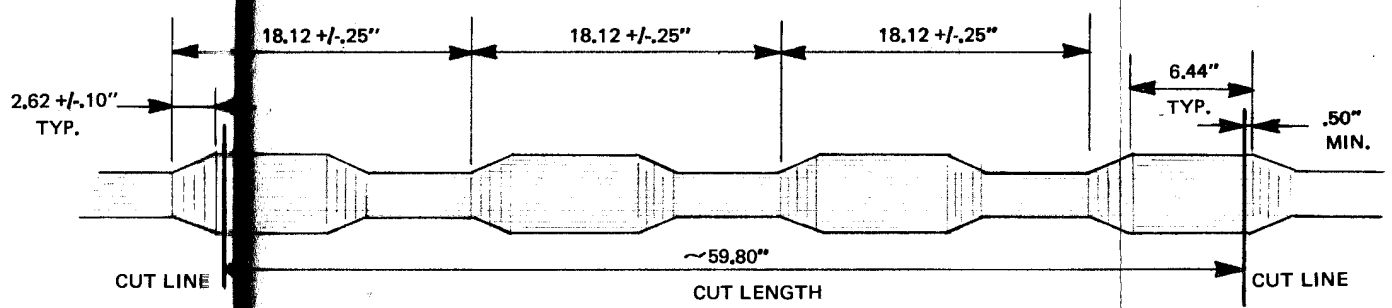
BISHOP GRAPHICS, INC.
REORDER NO. 20621

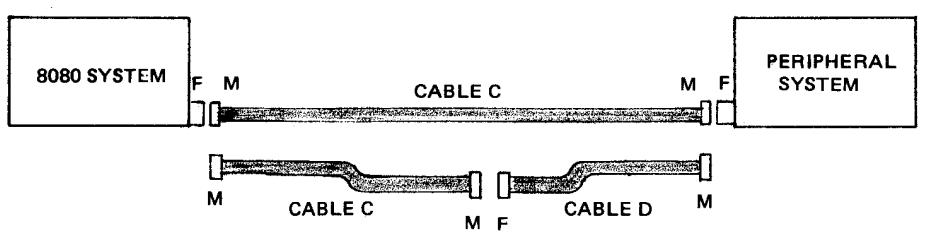
REVISIONS				
LTR		DESCRIPTION	DATE	APPROVED
0	ORIGINAL		10/76	D. Lanoll





JUNCTION SHELL/CONNECTOR DETAIL





INTER CHASSIS CONNECTOR DETAIL

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS ±	DEC. ±	ANGLES ±

APPROVALS	DATE
DRAWN PRU	10/25/76
CHECKED D. Lanoll	2/2/77

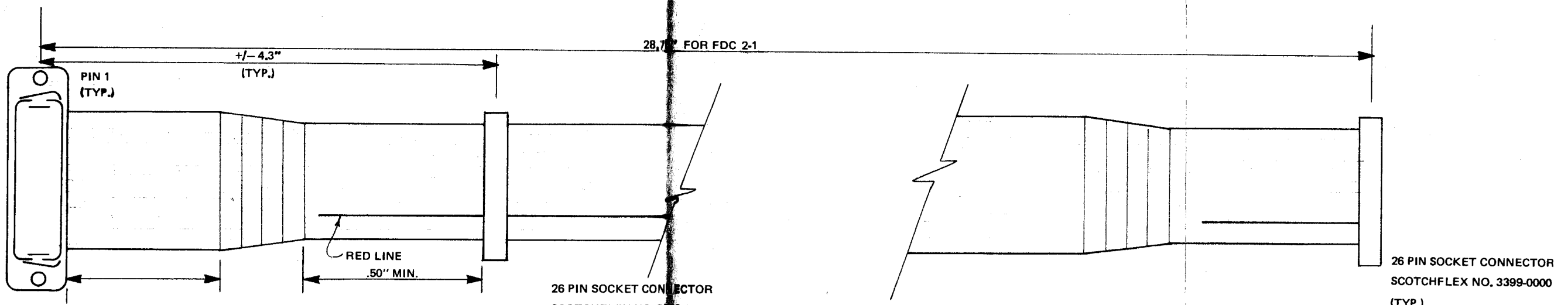
FLOPPY DISK SYSTEM
CABLE D
ASSEMBLY 91-0400005

SCALE	SIZE	DRAWING NO.
———	B	91-2040005

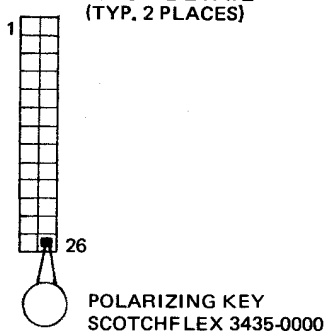
DO NOT SCALE DRAWING | SHEET

BISHOP GRAPHICS, INC.
REORDER NO 20621

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL	9/76	
1	MODIFIED	1/77	PRU



26 PIN SOCKET CONNECTOR DETAIL
(TYP. 2 PLACES)

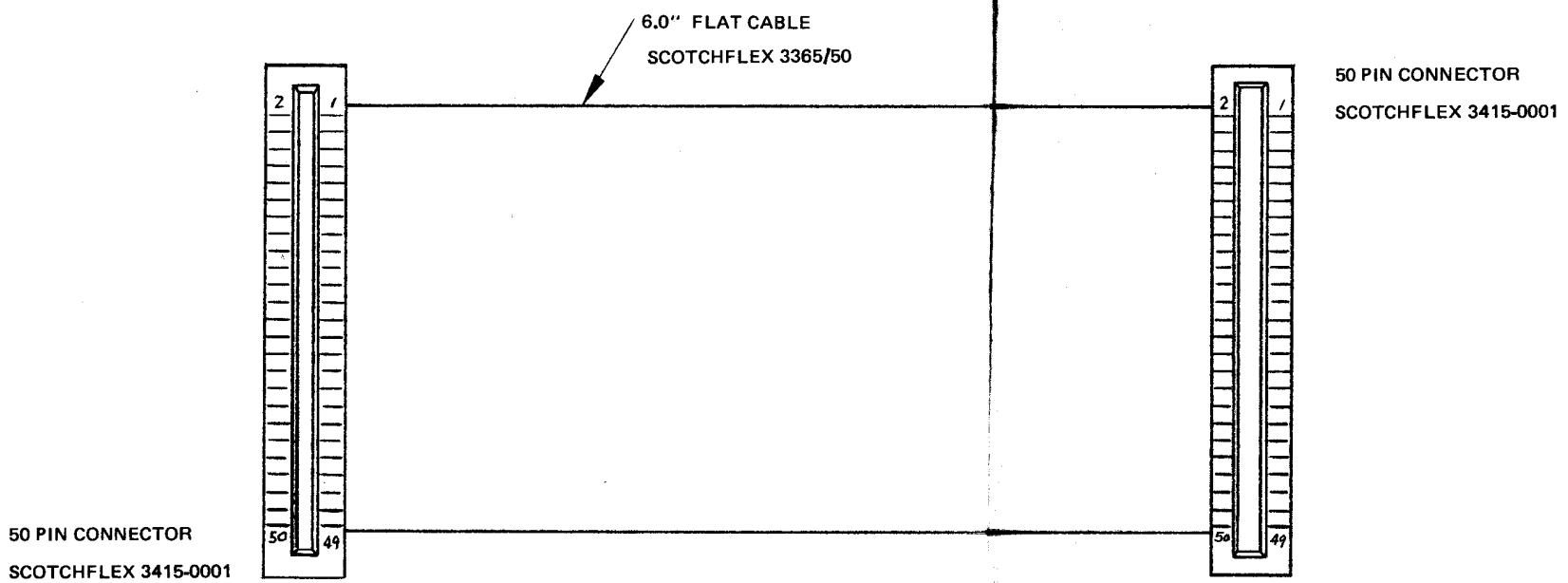


CABLE E FOR FDC 2-1

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS ± DEC. ± ANGLES ±	
APPROVALS / DATE	FLOPPY SYSTEM CABLE E ASSEMBLY 91-040006
DRAWN PRU 1/10/77	
CHECKED S. Carroll 2/2/77	SCALE / SIZE B / DRAWING NO. 91-2040006
	DO NOT SCALE DRAWING / SHEET

BISHOP GRAPHICS, INC.
REORDER NO. 20621

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ORIGINAL	6-22-76	S. Ahl...
1	REVISED TO INCLUDE PARTS CALLOUT & DWG Nº. INFO	9/13/76	D. Carroll



TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS ± DEC. ± ANGLES ±

APPROVALS	DATE
DRAWN J. C.	6-22-76
CHECKED S. Ahl...	6-22-76

FLOPPY DISK SYSTEM
CABLE F
ASSEMBLY

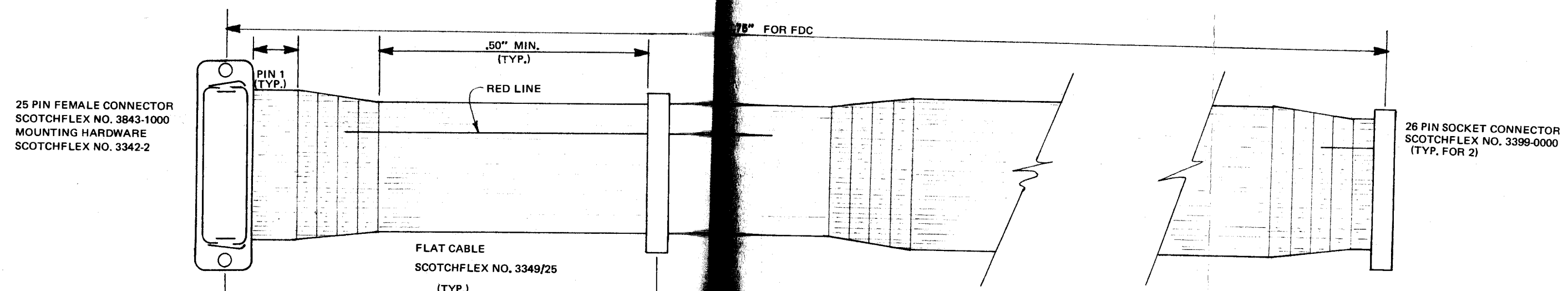
91–0400007

SCALE	SIZE	DRAWING NO
———	B	91–2040007

DO NOT SCALE DRAWING — SHEET 1 OF 1

BISHOP GRAPHICS, INC.
REORDER NO. 20621

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL	9/76	
1	MODIFIED	1/77	PRW



26 PIN SOCKET CONN[illegible]AIL
(TYP. 2 PLAC[illegible]
PIN 1

[illegible]Y
435-0000

CABLE T FOR FDC

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC. ANGLES ± ± ±		
APPROVALS / DATE	FLOPPY SYSTEM CABLE T ASSEMBLY	
DRAWN PRW 1/10/77		91-0400021
CHECKED D. Carroll 2/2/77	SCALE	SIZE B / DRAWING NO. 91-2040021
DO NOT SCALE DRAWING		SHEET

APPENDIX A

CALCOMP

140 FLOPPY DISK DRIVE

OEM REFERENCE MANUAL

1975 EDITION