BYTE FRONT PANEL BOARD

FUNCTIONAL DESCRIPTION

The Byte Front Panel Board provides a unique hardware breakpoint or stop on compare of address switch function for the operator with control of the BYT-8 computer (or any similar S-100 system). See Figure 1. below. The Front Panel Board provides buffering for all the front panel switches and receives the information to be displayed by the LED's on the front panel. The CPU control circuits are located on this board. The board also provides

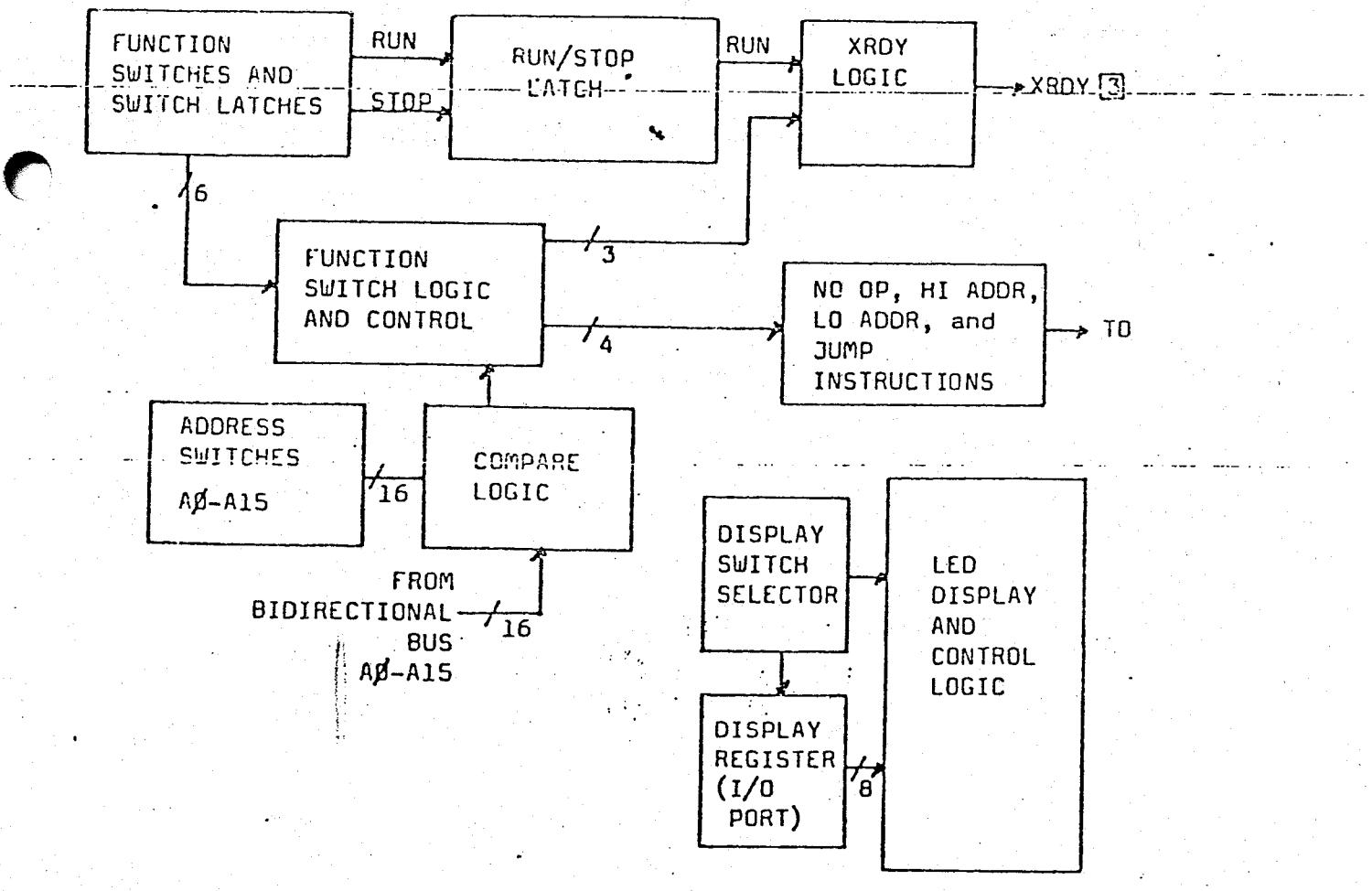


FIGURE 1. BYT-8 Front Panel Board Simplified Block Diagram

selectively display 16-bits (two 8-bit bytes) of Machine Address, one byte of CPU Status and one byte of CPU Data, one byte of Machine State and one byte of I/O Port Data, protect or not protect the contents of memory (if a RAM card is used), examine and/or modify the contents of memory, set or reset the RUN latch, single instruction step, stop on any OP code Address Compare, and Input Port can sense eight switches (front panel), reset front panel and CPU, or reset entire system except the CPU.

THEORY OF OPERATION

Before going into a detailed theory of operation, several basic circuits will be covered: the Latch, Exclusive OR Gates, DOT-OR or Wired-OR Gates, and 3-State Logic.

Latch Circuit Description (see Figure 2.)

Initial Conductions: pin 3 is low (0) and pin 7 is high (1).

SET: $\overline{\text{SET RUN}}$ goes low (0), causing pins 3 and 4 to go high (1). If pins 5 and 6 are high (1), then pin 7 can go low (0) and hold pin 2 low (0). Now pin 1 can go high (1) but the latch will remain set (pin 3 high and pin 7 low).

RESET: If either $\overline{\text{RESET}}$ or $\overline{\text{SET STOP}}$ go low (0), then pin 7 can go high (1), holding pin 2 high (1). This will cause pin 3 to go low (0) and hold pin 4 low (0). The latch is now in the reset condition (pin 3 is low and pin 7 is high) and will remain in this state until the next $\overline{\text{SET RUN}}$ signal goes low (0).

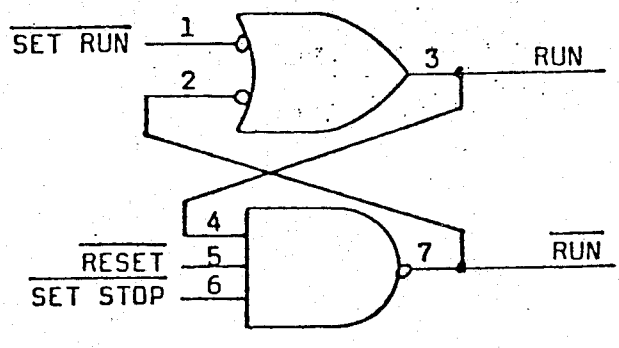
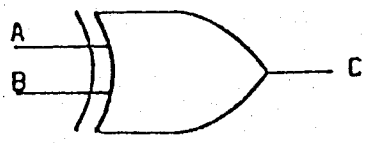


FIGURE 2. Latch Circuit Diagram

Exclusive OR Gate Symbol and Truth Table (see Figure 3.)

The inputs to the Exclusive OR Gate can not be the same or the output will be a low (0). This is shown in the Truth Table.



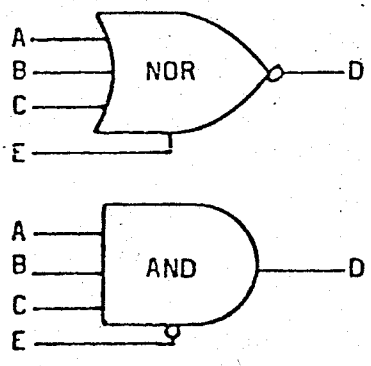
TRUTH TABLE

Input		Output	
A	B	C	
0	0	0	A + B = C
1	0	1	
0	1	1	
1	1	0	

FIGURE 3. Exclusive OR Gate

3-State Logic Descriptions (see Figure 4.)

The 3-State logic family contains an inhibit gate in the output line that must be enabled before the output can be set to a high or a low. If the inhibit gate is not enabled, the output will appear to be open. This condition can be used to an advantage when several open collector gates are to be used with a common pull-up resistor and each gate is enabled at a different time.



TRUTH TABLES

NOR					AND				
A	B	C	E	D	A	B	C	E	D
0	0	0	1	1	0	0	0	0	0
0	0	0	0	X	0	0	0	1	X
1	0	0	0	X	1	1	1	1	X
1	1	1	1	0	1	1	1	0	1
0	1	1	1	0	1	0	1	0	0
0	0	1	1	0	0	1	1	0	0
0	1	0	1	0	1	0	1	0	0

X = OPEN

FIGURE 4. 3-State Logic Symbols and Truth Tables

DOT-OR or Wired-OR Configuration (see Figure 5.)

The DOT-OR or Wired-OR configuration uses 3-State NOR gates or OR gates or a combination of both gates. NOR gate A is enabled when Ø1 goes high, thus

goes high, Ø1 is low and Ø3 is high, the output signal appears at pin 8. Likewise, when Ø3 goes low and Ø1 and Ø2 are low, the output signal appears at pin 9. The enabling input can be either a high or a low, depending on the logic element being used. If two of the gates should be enabled at the same time, it would be difficult to determine which input was causing the output. This could present some problems. Therefore, make sure that one and only one gate is enabled at a time when using this type of circuit.

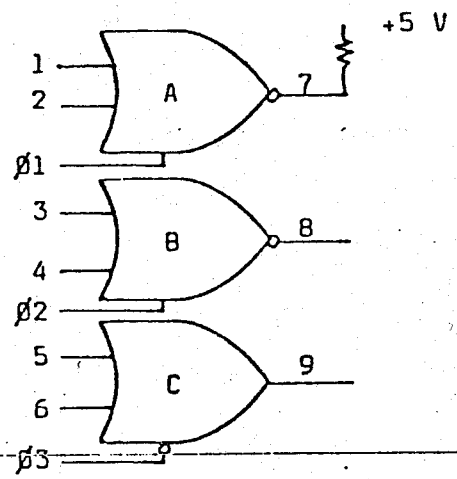


FIGURE 5. DOT-OR or Wired-OR Configuration

General

The six Front Panel function switches (S17-S22) allow the operator to control the CPU. The CPU is controlled by the XRDY line 3, the SS (Single Step) line 21, and the RUN line 71, all of which are produced from the Front Panel Board. Refer to the Front Panel Switches and Displays photograph and the Overall Schematic Diagram.

RUN/STOP Functions (see Figure 6.)

The RUN/STOP switch, S17, controls the XRDY line through the RUN/STOP latch. The RUN/STOP latch is actually two separate latches (RUN and STOP) that are interconnected to produce the RUN/STOP latch functions. The RUN function is initiated by setting the RUN/STOP switch to the RUN position. This generates a negative 100us pulse ($\overline{\text{SET RUN}}$) that is applied to D1 pins 4, 5, and 6 and to B6 pin 2. The negative going edge of the pulse from D1 pin 8 triggers

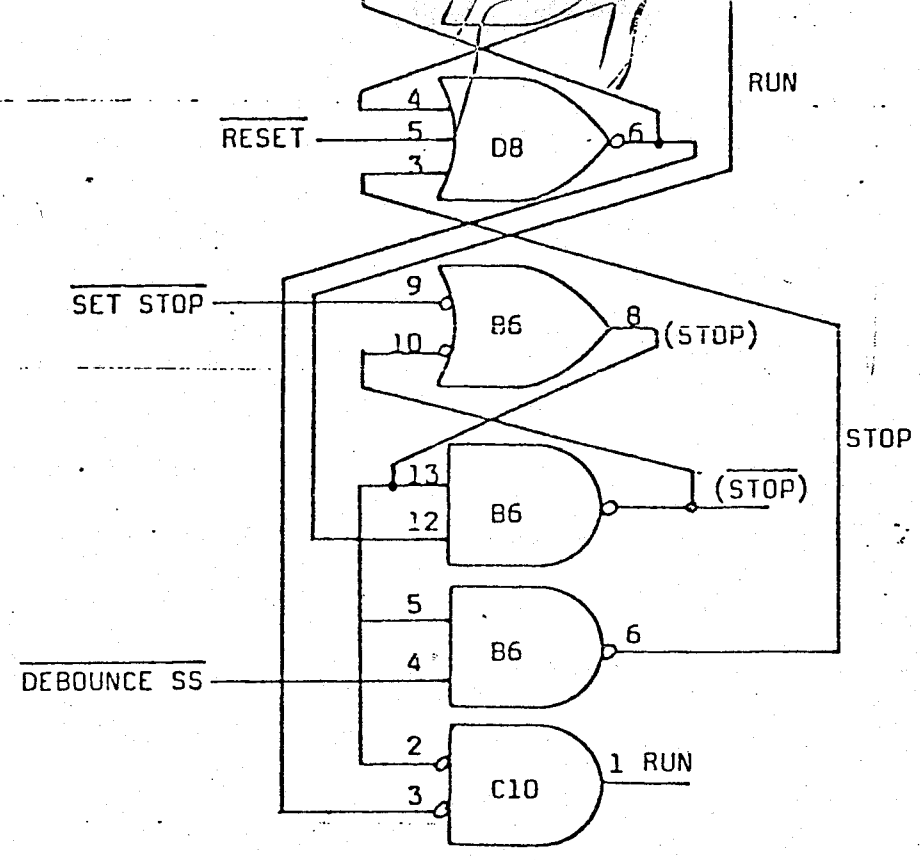


FIGURE 6. RUN/STOP Latch Simplified Schematic

a 3 ms negative pulse from C5 pin 4 ($\overline{\text{DEBOUNCE SS}}$). The low signal ($\overline{\text{SET RUN}}$) at B6 pin 2 causes B6 pin 3 to go high and hold D8 pin 4 high. D8 pin 5 is held high because $\overline{\text{RESET}}$ is high at this time. D8 pin 3 is held high because B4 pin 4 ($\overline{\text{DEBOUNCE SS}}$) is low, forcing B6 pin 6 to go high. B8 pin 6 is low and B6 pin 1 is held low, the RUN latch is now set and the low ($\overline{\text{SET RUN}}$) input signal at pin 2 can be removed without affecting the latch. The low at D8 pin 6 causes C10 pin 3 to be low. The low at B6 pin 8 (STOP) holds C10 pin 2 low and this allows C10 pin 1 (RUN) to go high. The high from C10 pin 1 is inverted at B10 pin 2 ($\overline{\text{RUN}}$) and applied to C6 pin 1. If the Front Panel is not in an Examine, Examine Next, or STEP function, the other three inputs to C6 will be low and C6 pin 6 will go high. This signal is buffered by B8 and produced at B8 pin 5 (XRDY, bus pin 3). The high on the XRDY line puts the CPU into a RUN operation. The $\overline{\text{DEBOUNCE SS}}$ signal at B6 pin 4 goes high after 3 ms delay but B6 pin 5 remains low, holding B6 pin 6 high. The

RUN/STOP latch will remain set until the SET STOP or the RESET signal goes low.

The STOP function is initiated by setting the RUN/STOP switch, S17, to the STOP position. This generates a negative 100us pulse that is applied to D4 pin 13 and causes D4 pin 11 to go high. This high is applied to C6 pin 9. C6 pin 10 is high (PSYNC), pin 12 is high (Ø2), and pin 13 (SM1, Machine Cycle 1 - fetch cycle) is high. So C6 pin 8 goes low ($\overline{\text{SET STOP}}$). This signal causes B6 pin 8 (STOP) to go high and holds B6 pins 5 and 13 high and C10 pin 2 high. B6 pin 11 goes low and holds B6 pin 10 low, setting the STOP latch. B6 pin 6 can now go low and cause D8 pin 6 to go high and reset the RUN latch. The high on D8 pin 6 inhibits the RUN signal (C10 pin 1). The RUN/STOP latch will remain in this state, $\overline{\text{SET RUN}}$ signal is received at B6 pin 2, and the RUN/STOP latch cycle starts over.

Examine Function

The Examine function is initiated by setting switch S22 (EXMN/ENXT) to the EXMN position, generating a 100 ms negative-going pulse that is applied to C1 pin 1 and D1 pin 12. The positive-going pulse at D1 pin 8 triggers a 3 ms pulse from C5 (a monostable flip-flop) on its negative transition. The 3 ms pulse removes the low (0) from the latch circuits and allows C1 pin 6 to go low (0). This 3 ms time delay removes any switch bounce from the output signal. The low signal from C1 pin 6 is applied to D3 pin 2. B9 pins 9 and 10 are held high by the $\overline{Q}$ outputs of C7 pins 2 and 6. The low output of B9 pin 8 is applied to D3 pin 3, allowing the output pin 3 to go high. The high output of C9 pin 12 holds the output of D3 pin 4 low. The input at D3 pin 12 causes the output (pin 13) to go low. This negative transition applied to C7 pin 12 causes the J-K flip-flop to toggle, causing the Q and $\overline{Q}$ outputs to change state (pin 3 is high and pin 2 is low). The two J-K flip-flops are connected as a Two Bit Counter (four states). The change

in the outputs of the first flip-flop has no effect on the second flip-flop. But the input to B9 pin 10 is now low and the output of B9 pin 8 is high, causing pin 1 of D3 to go low and C9 pin 12 to go low and hold pin 6 of D3 low. The high at C7 pin 3 (Q) is applied to C7 pin 9 and to D9 pins 5 and 10. The high at C7 pin 6 is applied to D9 pin 9 and to B9 pin 9. The PDBIN signal at C9 pin 6 goes high and is applied to D9 pin 11, causing D9 pin 8 to go low and C4 pin 10 to go high (JMP). This enables the JUMP instruction (C3 HEX) to be applied to the bidirectional bus through J1 via the inverters in B17 (pins 1, 9, 11, and 13).

The PSYNC signal (76) is inverted at B7 pin 2, buffered by B8, and applied to various circuits from B8 pin 3 as $\overline{\text{PSYNC}}$. $\overline{\text{PSYNC}}$ is applied to D3 pin 5 and with pin 6 held low, the output (pin 8) goes high. This pulse going positive causes D3 pin 13 to go low and trigger the J-K flip-flop (C7) a second time. This causes the output at pin 3 to go low and at pin 2 to go high. The low going signal from pin 3 causes the second J-K flip-flop to change state, pin 5 goes high and pin 6 goes low. The change in the outputs of the flip-flops causes D9 pin 8 to go high, inhibiting the JUMP instruction (C3 HEX). D8 pins 2 and 3 are held high so the next PDBIN signal causes D8 pin 12 to go low and puts the $\overline{\text{GATE LO ADDRESS}}$ signal from C8 pin 8 on A16 pins 1 and 15 and on B16 pin 15. This allows the eight low address bits (AØ through A7) to be placed on the bidirectional bus by the 74367's. The 74367's are 3-state logic 6-bit noninverting buffers (see the description of 3-state logic).

The second $\overline{\text{PSYNC}}$ pulse causes C7 pin 12 to go low and change the output states a third time, pin 3 goes high and pin 2 goes low. The second J-K flip-flop does not change state, so pin 5 remains high and pin 6 remains low. D8 pin 12 goes high, inhibiting the $\overline{\text{GATE LO ADDRESS}}$ signal. D9 pins 3 and 5 are high and the next PDBIN pulse causes pin 6 to go low and the

eight high addresses (A8 through A15) to be applied to the bidirectional bus.

The third $\overline{\text{PSYNC}}$ pulse again causes the trigger input of C7 (pin 12) to go low and change the state of the outputs, pin 3 goes low and pin 2 goes high. The change of state at pin 3 causes the second J-K flip-flop to change state, pin 5 goes low and pin 6 goes high. Both J-K flip-flops are back to their original states. The $\overline{\text{GATE HI ADDRESS}}$ is inhibited when D9 pin 6 goes high.

The Examine Function logic has provided the CPU with a JUMP instruction and the two address bytes (high and low) that the CPU expects after a JUMP instruction. The CPU is halted during the fetch routine for the addressed memory byte.

Deposit Function

The Deposit function is initiated by setting switch S21 (DEP/DNXT) to the DEP (Deposit) position, generating a 100 ms negative-going pulse that is applied to D1 pin 2 and to C3 pin 13. The positive-going pulse at D1 pin 8 triggers a 3 ms pulse from C5 pins 4 and 13 on its negative transition. The 3 ms pulse removes any switch bounce from the output of the latches. The low at C3 pin 8 is applied to C8 pin 1 and C8 pin 2 is held high. Therefore, the output of C8 (pin 3) goes low and triggers D2 (J-K flip-flop) that has been reset by C5 pin 13 returning to a low. D2 pin 3 is now high and is applied to D4 pins 10 and 15. D2 pin 6 is set high by the last $\overline{\text{PSYNC}}$ pulse and is applied to D4 pin 9. The output of D4 (pin 2) goes low and triggers a 15 ms negative pulse from C5 pin 12. This pulse is applied to B9 pin 2. Pin 1 of B9 is the $\overline{\text{PWR}}$ signal (Processor Write). The output of this gate is ANDed with C8 pin 4 ($\overline{\text{SOUT}}$) to produce the MWRITE signal (68). The PWAIT (27) signal at D4 pin 4 causes D4 pin 6 to go low. This

Pin 8 of C8 goes low, producing the GATE LO ADDRESS signal to apply the eight bits of data to the bidirectional bus. D8 prevents the CPU from applying data on the bidirectional bus while the Front Panel is inserting data. The inputs to D8 are as follows: pin 1 — $\overline{\text{GATE DATA}}$, pin 10 — the output of B9 pin 8 is low only during the time that both C7's flip-flops are reset, and pin 9 — low only when D2 pin 9 has been triggered and pin 8 is high (this occurs during either the Examine Next or Deposit Next Function). The output of D8 (pin 8) then goes high causing B7 pin 10 to go low, holding both (21) and (71), SS and RUN, low.

Examine Next Function

The Examine Next function is initiated by setting the EXMN/ENXT switch S22 to the ENXT position. This produces a low at C1 pin 8 after a 3 ms delay as previously described. This low is applied to C2 pin 10 and causes a high from C2 pin 8. This high is inverted by B7 and applied to D2 pin 9. If the processor is halted, pin 8 of D2 will be high ($\overline{\text{RUN}}$) and pin 6 will go low. The signal from pin 6 is applied to D3 pin 9 and to C6 pin 4. D3 pin 10 goes low with the next $\overline{\text{PDBIN}}$ signal to produce a NO OP instruction (000 HEX) to be applied to the bidirectional bus and to gate out the XRDY signal from C6 pin 6. $\overline{\text{PSYNC}}$ resets D2 pin 6 to a high on the next pulse. This removes the low on D3 pin 9 and removes the NO OP instruction from the bus.

Deposit Next Function

The Deposit Next Function is initiated by setting the DNXT/DEP switch S21 to the DNXT position. After a 3 ms delay, a high is produced at pin 3 of C2 and a low at pin 6 of C2. The low at pin 2 is applied to pin 9 of C2. This signal follows the same path as the Examine Next Function previously described, generating a NO OP instruction and gating out the XRDY signal. The high from pin 3 follows a different path and generates different signals. The

causing pin 11 of C2 to go low. This low going pulse is ORed through C8 and applied to D2 pin 12. The low going edge triggers the J-K flip-flop, if pin 1 ($\overline{RUN}$) is high. This causes the output of D2 (pin 3) to go high. The signal at pin 3 is applied to D4 pins 5 and 10. The signal at pin 4 of D4 is PWAIT and causes D4 pin 6 to go low, producing the $\overline{GATE\ DATA}$ signal. This signal is applied to C8 pin 10 to generate the $\overline{GATE\ LO\ ADDRESS}$ instruction that enables A16 and part of B16. The $\overline{GATE\ DATA}$ signal is also applied to D8 pin 11 to hold SS and RUN signals low.

When D2 pin 6 is high and D2 pin 3 is high, D4 pin 2 goes low, triggering a 15 us negative pulse from C5 pin 12. This signal produces the MWRITE signal when gated with $\overline{PWR}$ and SOUT signals as described in the Examine Next Function description. The next PSYNC signal inhibits the NO OP instruction by resetting D2 pin 10.

Step Function

The Step function is initiated by setting the STEP/CMPR switch, S20, to the STEP position. After a 3 ms delay, C3 pin 6 goes low, causing C4 pin 6 to go low, if pin 8 ($\overline{RUN}$) is high. The signal from pin 6 is $\overline{STEP}$. This is applied to C6 pin 2 to produce the XRDY signal. The next PSYNC signal resets C4 pin 6 to a high.

Set Compare Stop Function

The Set Compare Stop function is initiated by setting the STEP/CMPR switch, S20, to the CMPR position. The switch closing produces a negative going pulse at C4 pin 12, that causes C4 pin 3 to go high. This high is applied to D4 pin 2. D4 pin 1 is high when D15 pin 8 goes low, and B10 pin 12 goes high when the programmed and selected addresses compare. Then pin 3 of D4 goes low and is applied to D4 pin 12. D4 pin 11 goes high and is applied to C6 pin 9. C6 pin 10 is PSYNC, pin 12 is Ø2 clock, and pin 13 is SM1 (Machine

producing the $\overline{\text{SET STOP}}$ signal, that is used to set the RUN/STOP latches to STOP. When the latch is set to stop, the $\overline{\text{STOP}}$ signal from B6 pin 11 resets C4 pin 3 to a low.

Input/Output Port Functions

The upper eight switches (A8-A15) are used for the address of the I/O Port functions. The upper switches are also used as sense switches. The inputs to C11 are the eight upper addresses (A8-A15 or FF HEX), when all eight are C11, pin 8 is low ($\overline{\text{ADDR=FF}}$). This signal is applied to C9 pin 9, inverted and available at pin 8. The signal from pin 8 is applied to D9 pin 13. It is ANDed with SINP on pin 13 and with PDBIN on pin 1. When all three signals are high, pin 12 goes low. This produces the $\overline{\text{SSWDSB}}$ signal (Status Word Disable), (53), that is gated to prevent timing problems on the bidirectional bus from the CPU and the Front Panel Board. The other place that this signal is applied is to C8 pin 12. This signal causes pin 8 to go low and produce the Gate Hi Address signal. The Gate Hi Address signal enables A15 and B16 bus drivers. This allows the upper address switches to be put on the bi-directional bus without interference from the CPU.

The signal from C11 pin 8 ($\overline{\text{ADDR=FF}}$) is applied to C10 pin 6 and is ANDed with $\overline{\text{SOUT}}$. When both signals are low, pin 4 goes high and B10 pin 8 goes low. This signal holds C10 pin 9 low. C10 pin 8 goes low when $\overline{\text{PWR}}$ (Processor Write) is low. This causes pin 10 to go high and applies a high to C15 pin 11 (Strobe). With the DISPLAY SELECTOR switch (S16) in the center position, B9 pin 11 is low and holds C15 pin 13 high. When pin 13 is high, the eight outputs of C15 are enabled. The high at pin 11 latched in the data from the eight input lines. Whenever the DISPLAY SELECTOR switch is in either the up or down position, B9 pin 11 will be high, forcing C15 pin 13 low, disabling the eight outputs of C15.

1 and 15, and D11 pins 1 and 15 are enabled so the 16-bits of address are displayed (AØ-A15). When the DISPLAY SELECTOR is in the center position, B9 pin 11 is low and C15 pin 12, D13 pin 15, and D10 pins 1 and 15 are enabled so that 8-bits of state and 8-bits of I/O Port are displayed. When the DISPLAY SELECTOR is in the up position, C12 pin 15, C16 pin 1, D13 pin 1, and D14 pins 1 and 15 are enabled so that 8-bits of data and 8-bits of status are displayed.

Reset/Clear Functions

The Reset/Clear functions are initiated by setting S18 to the desired position. The RESET position forces the $\overline{\text{RESET}}$ line low (75), resetting C5, C7, the RUN/STOP latch, and C15. The signal is also applied to the CPU where it resets the program counter to 0 000 000 000 000 000, the first memory address. This is a quick way to get back to the first step of a program, if it begins at the first memory address. The CLEAR position produces the same effect as the RESET position, with the extra function that it will clear all the external input and output devices. Whenever the switch (S18) is set to RESET, a CLEAR signal is produced because of the diode (CR1) connecting the $\overline{\text{RESET}}$ line to the $\overline{\text{CLEAR}}$ line.

Protect/$\overline{\text{Protect}}$ Functions

The Protect/$\overline{\text{Protect}}$ functions are initiated by setting S19 to either desired position. In the PROTECT position, when $\overline{\text{RUN}}$ is high, the PROTECT line (70) is set high; this signal is applied to the memory protection circuits and prevents any change in the contents of memory. When the switch is set to the $\overline{\text{PROTECT}}$ position, when $\overline{\text{RUN}}$ is high, the $\overline{\text{PROTECT}}$ line (20) is set high; this will disable the memory protection circuits and allow the memory contents to be changed.

The MOS IC in this kit requires special handling precautions. To prevent damage to the MOS IC, read and follow the precautions listed below.

1. Keep all equipment at the same potential as the PC board, work surface, and the IC itself. This is accomplished by continuous physical contact with the work surface, PC board, etc.
2. Always touch the metal container first, before touching the IC itself.
3. Handle the IC by the front and rear edges, not by the pins on either side.
4. If the IC is to be transferred from one container into another, touch the metal containers together before transferring the IC.
5. Touch the PC board before inserting the IC into the board or its socket and maintain contact until the IC is installed.
6. Never touch anything to the IC that has not been handled by you first.
7. Wear cotton clothing, if possible, to reduce static charges, rather than wool or synthetic fabric.
8. Avoid placing the IC near plastic, as dry air, moving over the plastic, can develop high static charges.

Assembly Hints

Soldering — Only resin-core solder should be used. Use a fine soldering tip and a low-wattage element, approximately 15 to 25 watts. Keep the tip clean and well tinned. Clean the tip on a damp sponge. Apply heat to the joint to be soldered, then apply solder to the joint, not to the tip. Remove heat from the joint, being careful not to disturb the solder joint. DO NOT apply heat for a long period of time. This could damage or destroy some of the components (MOS IC's, transistors, diodes, etc.) or lift traces or pads. A good solder joint appears smooth and shiny. Too much heat or moving the

problems that are very difficult to find. If you wish to install sockets for all of the IC's, they are available at the nearest BYTE SHOP.

Component Placement — For a professional appearance, align all the color coding bands in the same direction (left or down). This will make finding a component value much easier once the board is assembled. Clip off all excess leads protruding from the board after soldering.

Board Assembly

Compare the received parts in the kit with the parts list before starting the assembly. Wash the board in warm water and detergent with a soft brush; this will remove any oil, dirt, etc. that may have accumulated on the board. Rinse the board with warm water and then rinse it with alcohol or a similar solvent to remove the water and detergent.

Mount the cleaned pc board, component side up (pins 1 and 50 will be visible on the 100-pin connector) on top of several layers of cardboard. This allows the component's leads to penetrate the cardboard and hold the components in place. Follow the figures in the Assembly Section for the proper sequence of installing the components.

1. Install resistors per Photo 1.
2. Install diode and all capacitors per Photo 2.
3. Install and solder regulator, heat sink, sockets and IC's per Photo 3. Additional sockets may be obtained from your nearest BYTE SHOP.

Stop the assembly at this point and check for shorts and solder bridges around the IC sockets, voltage regulators, and the 100-pin connector. Wash off the solder flux with alcohol or a similar solvent to get a clear view. When the board is clean, take an ohmmeter and check for shorts between each of the pins 1 through 100, then check the pin pairs for shorts (pins 1 and

pins 1/51 (+8 vdc) and pins 50/100 (ground). Then check for shorts between the +5 vdc line (Q1, pin 3) and ground. Complete the kit assembly by referring to Photos 4 and 5.

Board Cleaning

After completing all the soldering, scrub the trace side of the board with alcohol or a similar solvent and a stiff brush. Carefully wash the component side with alcohol and allow the board to dry. After washing and drying, inspect both sides of the board under a strong light for solder splashes, bridges, etc. Remove any particles that may be lodged between the traces. The board is now ready for checkout and use.

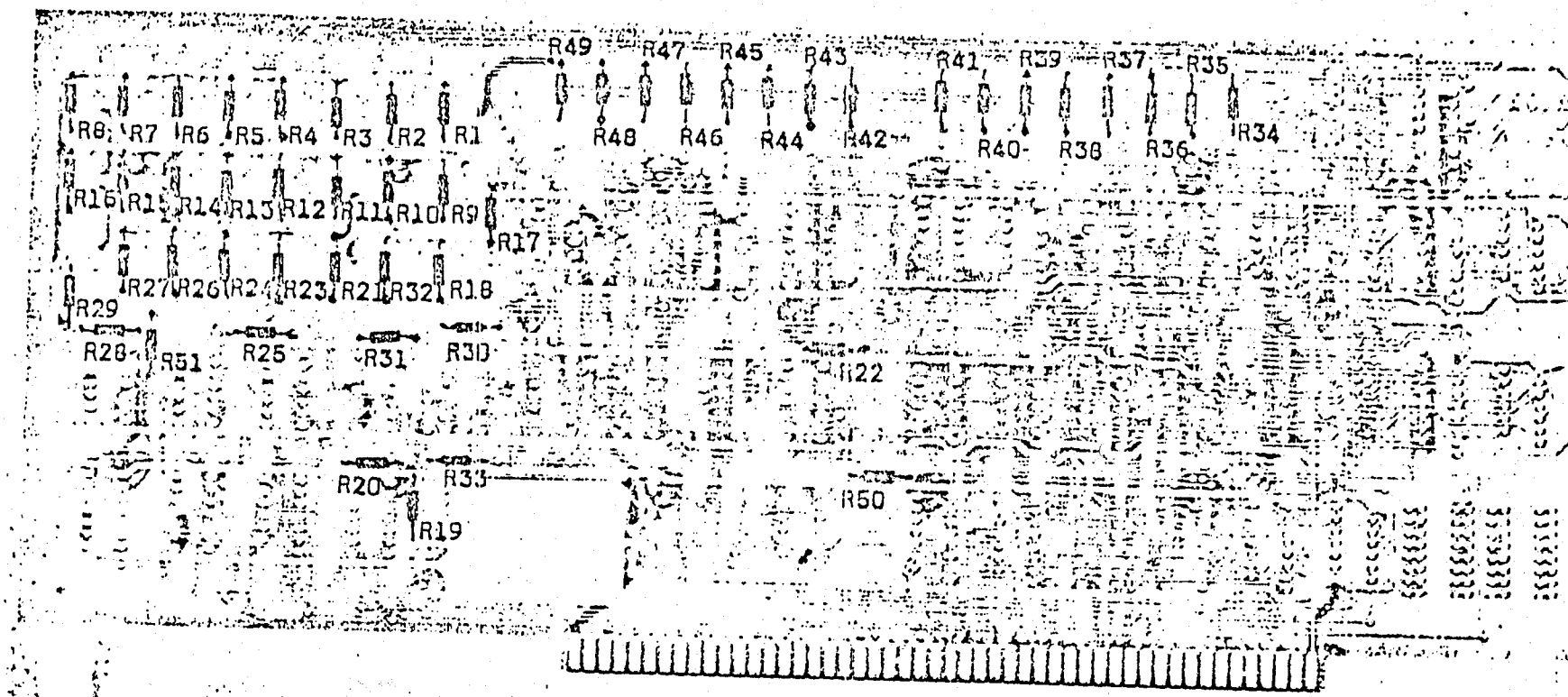


PHOTO 1 Install all resistors. 220 ohm R29; R34-R49; 1K R1-R16, R17, R18, R32, R21, R23, R24, R26, R27, R31, R25, R28, R20, R19, R50, R22; 47K R33; 100K R30; 270 K R51.

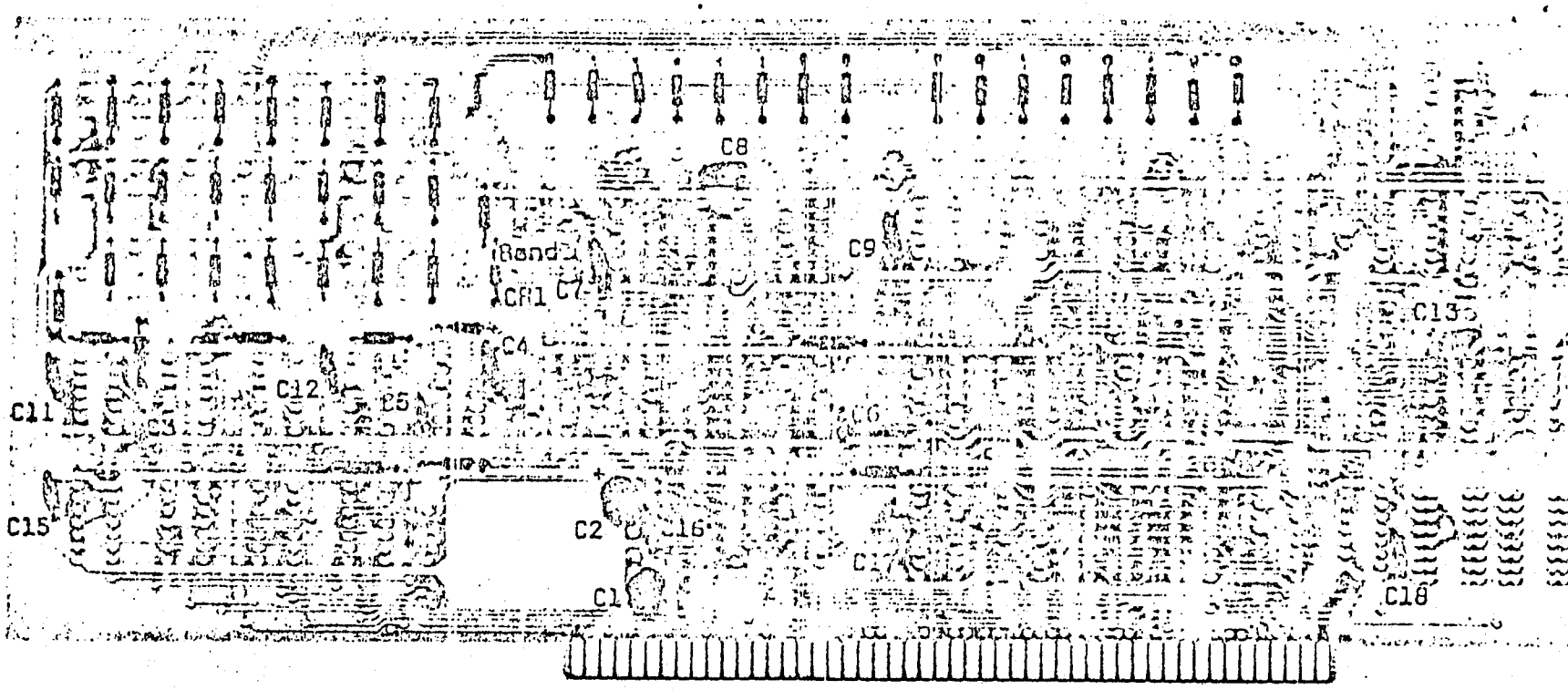


PHOTO 2 Install diode CR1 (note polarity). Install capacitors .001 uf, C5, C6. Install capacitors .1 uf, C3, C4, C7-C18. Install capacitors 33 uf, C1, C2 (tantalum) (observe polarity).

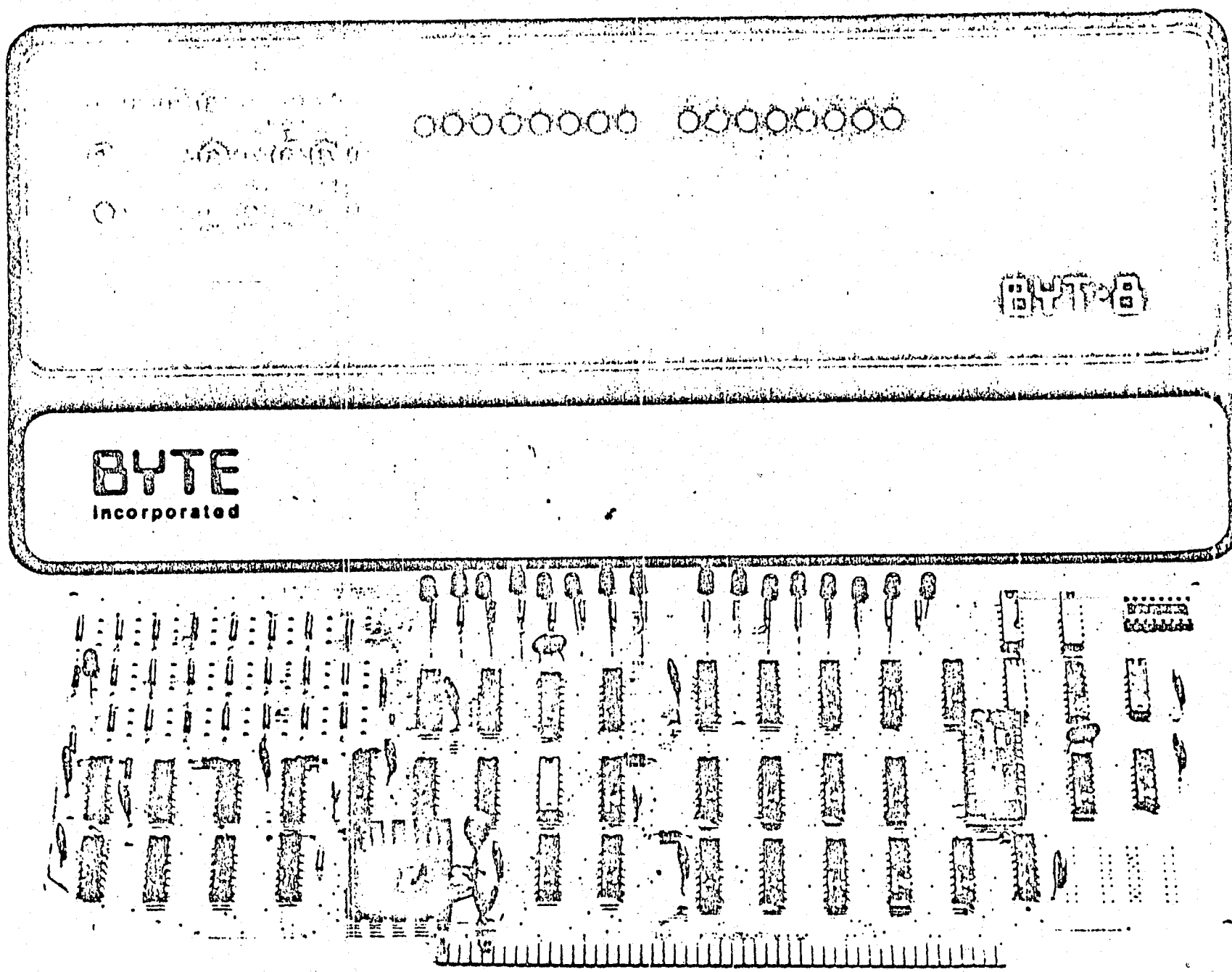


PHOTO 4 Insert LED's cathode side (flat side) toward the top of the board. DO NOT SOLDER. Install switches and LED collars on front panel: S0-S15 (ON-ON), S16 (ON-OFF-ON), S17-S22 (MOMENTARY).

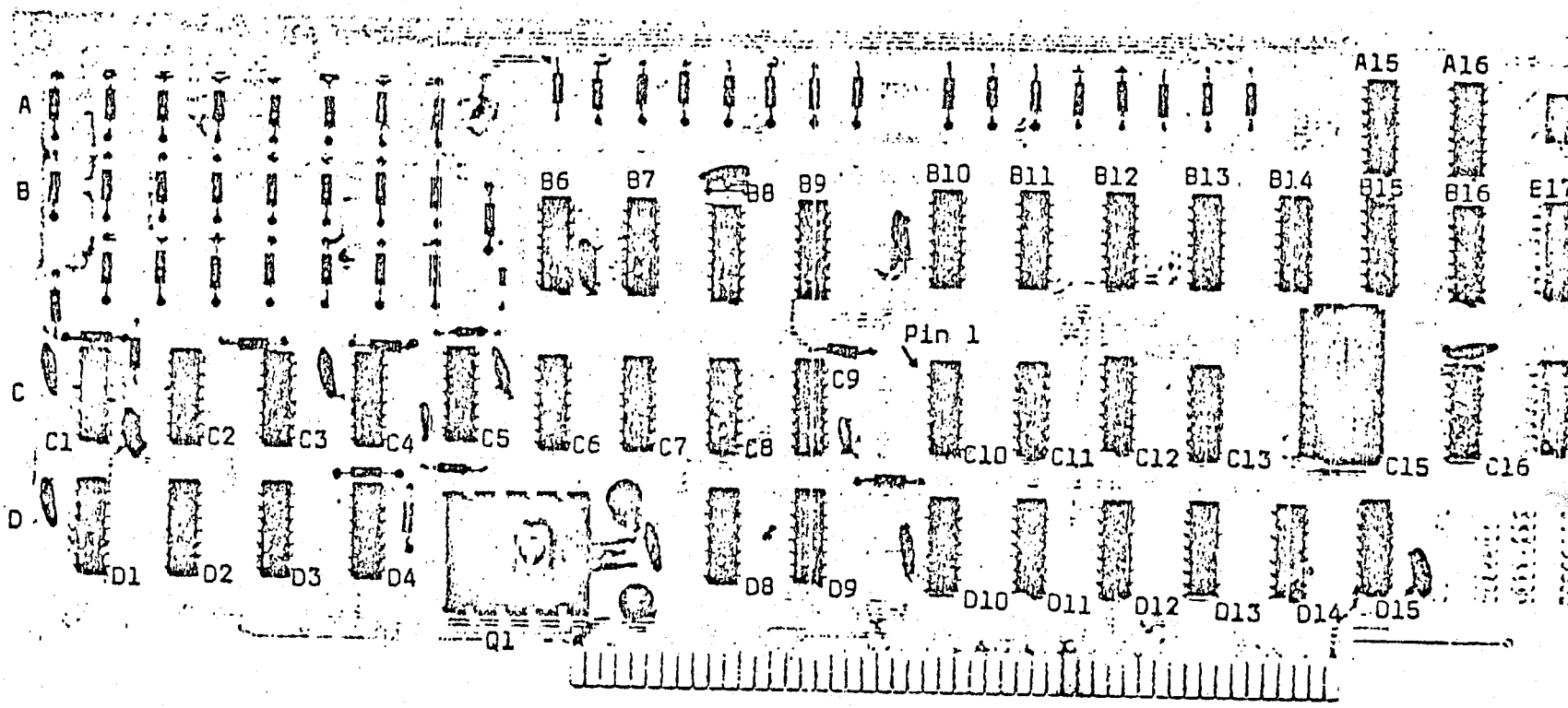


PHOTO 3 Install and solder regulator heat sink, sockets and IC's (note pin 1 designation). Refer to parts list for IC type. Additional sockets may be purchased at the BYTE SHOP.
Check for shorts as indicated on pages 14 and 15.
If optional front panel was purchased, follow assembly instructions presented on photos 4 and 5. Otherwise, go to photo 6.

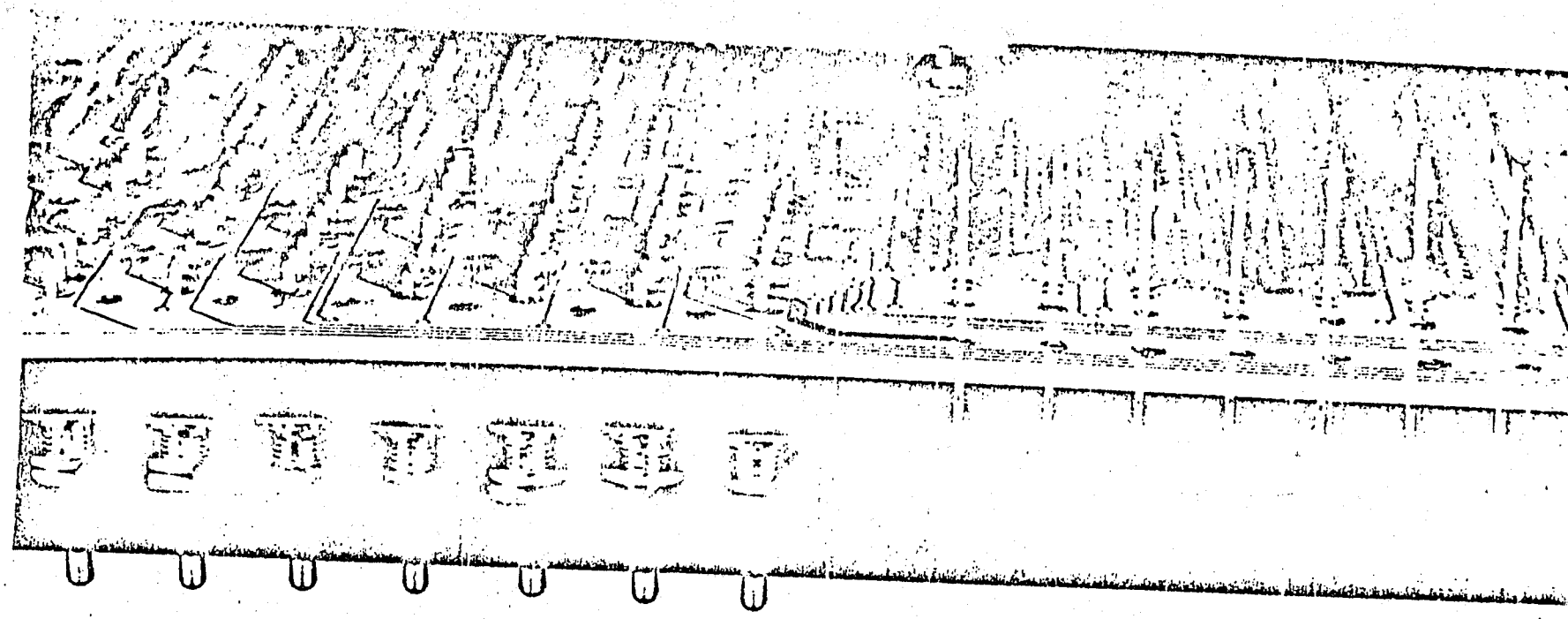


PHOTO 5

Note: When mounting switches to front panel, place back nut on third thread from bottom, install washer, insert switch in hole, and install nut on front [illegible].

Push LED's into collars using a pencil or other narrow object, then solder in place.

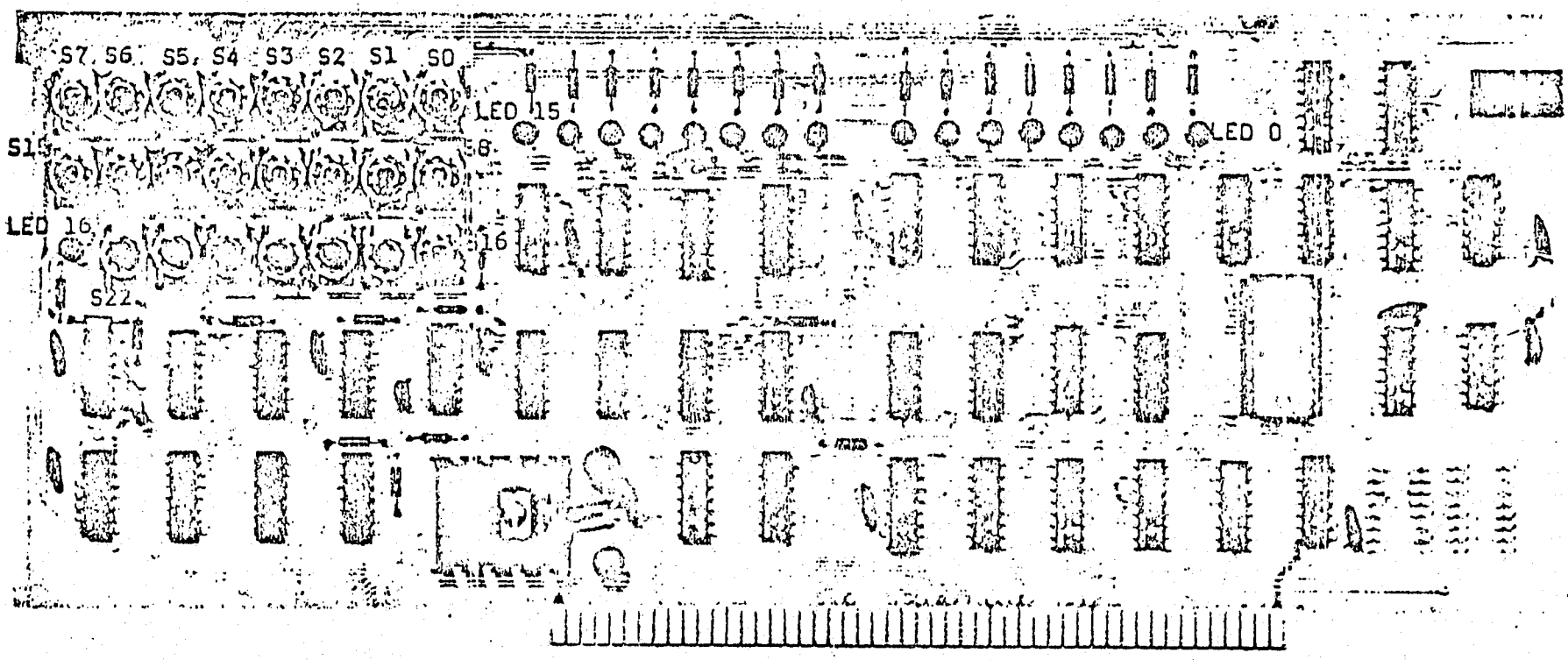


PHOTO 6 Insert and solder LEDs cathode side (flat side) at the top of the board. Install and solder switches: S0-S15 (ON-ON), S16 (ON-OFF-ON), S17 (MOMENTARY).

OPERATING INSTRUCTIONS

Power Up Instructions

Remove all other boards from the system. Insert the BYT-8 Front Panel Board into its connector with the system power off. Turn on the system power and measure the voltage at Q1 pin 3 (+5 vdc). Check the voltage at C15 pin 24 (+5 vdc). Check several other IC's for the proper voltages, as a confidence-builder. If all the voltages check out, turn off the system power and insert all the other boards into the system. Apply power to the system. If any problems arise, contact your nearest BYTE SHOP for assistance.

Checkout Instructions

Refer to the Front Panel photo and state and status description, pg. 24 and 25.

Reset — Set Reset/Clear switch to RESET position. Set Display Selector switch to down position. Address indication should be all indicators off.

Deposit — Set Display Selector to up position. Data indication (DØ-D7) will be whatever instruction happens to be in address location zero. Set data switches (SØ-S7) for the hexadecimal value (21) in the test program of Table 1. Set the DEP/DNXT switch to the DEP position. Data indicators (DØ-7) will now display the same information as the data switches. Set the data switches (SØ-S7) for the next hexadecimal value (FF) and set the DEP/DNXT switch to the DNXT position. Place the Display Selector switch down and check the address indicators (AØ-A15). For AØ on condition (this indicates you stepped from location zero to location one, and you have deposited instructions sequentially), place the Display Selector in the up position and continue putting the hexadecimal values of the test program in the data switches (SØ-S7) followed by a DNXT. (CAUTION: If the data indicators (DØ-D7) are not changing to the same value as the data switches, your Memory Board may be misaddressed or protected. To unprotect the board,

place the $\overline{\text{PROT}}$/PROT switch in the $\overline{\text{PROT}}$ position.) When the entire test program has been deposited into memory, place the Display Selector down and the Address indicators should have the value 002E Hexidecimal. If this is not so, you have erred when depositing the program into memory.

Examine — Place the Display Selector to the up position and put the Reset/Clear switch to the RESET position. The data indicators (DØ-D7) should display the contents of location zero (21 in test program). Put the EXMN/ENXT switch to the ENXT position and the data indicators should display the contents of location one (FF in test program). Continue depressing the ENXT switch and checking the display indicators for the proper value in the test program. If the contents of memory agree with the program listing in Table 1., you may proceed.

Run — Place all switches SØ-S15 down. Depress RESET switch, then depress RUN switch. If the Display Selector is in the up position, all the data indicators will appear on, as well as the appropriate CPU status. Put the Display Selector in the center position and the Output Port indicator (PØ-P7) will be turning on and off $P_7P_6P_1P_0$ then $P_2P_3P_4P_5$. The appropriate Machine State indicators will be on. Put the Display Selector down and the Address indicators will be flashing in an incremental fashion. You may now test STEP on Compare by putting an address value in SØ-S15 and depress CMPR. The AØ-A15 indicator should be the same value as SØ-S15. Depressing STEP will single step you through locations in memory. If you encounter problems with this test program, contact your BYTE SHOP.

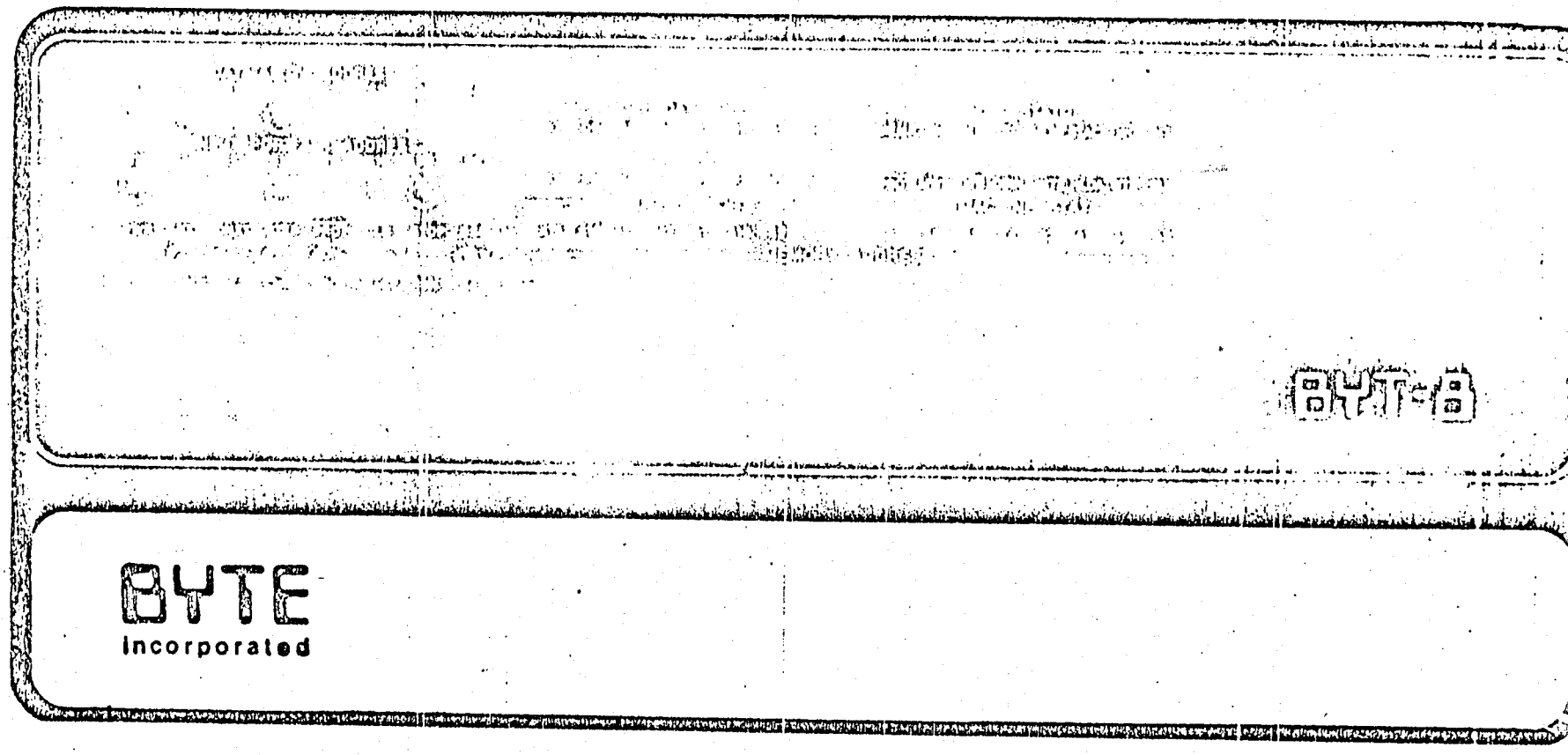


PHOTO 7 Assembled front panel and board.

STATUS AND STATE DESCRIPTION

	MEMR	= MEMORY READ OP
S	INP	= I/O INPUT OP
T	M1	= FETCH CYCLE OF FIRST BYTE OF INSTRUCTION
A	OUT	= I/O OUTPUT OP
T	HLTA	= CPU HALT CONDITION (REQUIRES INTERRUPT OR RESET TO START)
U	STACK	= STACK OPERATION
S	$\overline{WO}$	= WRITE MEMORY OR I/O OUTPUT
	INTA	= INTERRUPT ACKNOWLEDGE
	PROT	= ADDRESSED MEMORY IS PROTECTED
S	MWR	= MEMORY WRITE SIGNAL
T	$\overline{WR}$	= CPU WRITE SIGNAL TO I/O OR MEMORY
A	DBIN	= CPU DATA BUS GATED INBOUND (TO CPU)
T	INTE	= INTERRUPT IS ENABLED
E	HLDA	= CPU ACKNOWLEDGEMENT OF HOLD SIGNAL
	WTE	= CPU IS WAIT STATE

MEMORY ADDRESS DESCRIPTION (All Address Bits On = 65,536)

BIT:	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15
LOCATION.	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16384	32768

INPUT PORT
Senses switches S8-S15 on input instruction with FF address.

OUTPUT PORT
Displays output data in LED's PØ-P7 on output instruction with FF address.

CPU DATA BUS
Displays 8080 data bus in LED's DØ-D7 for each instruction.

LOCATION	DATA	INSTRUCTION
00	21	LXI H←FF
01	FF	
02	FF	
03	23	INX H
04	46	MOV B←M
05	7D	MOV A←L
06	EE	XRi FF
07	FF	
08	C2	JNZ→0003
09	03	
0A	00	
0B	7C	MOV A←H
0C	EE	XRi FF
0D	7F	
0E	C2	JNZ 0018
0F	18	
10	00	
11	3E	MVi A←C3
12	C3	
13	D3	OUT→IOFF
14	FF	
15	00	NOP
16	00	
17	00	

LOCATION	DATA	INSTRUCTION
18	7C	MOV A←H
19	EE	XRi FF
1A	FF	
1B	C2	JNZ→0003
1C	03	
1D	00	
1E	3E	MVi A→3C
1F	3C	
20	D3	OUT→IOFF
21	FF	
22	00	NOP
23	00	
24	00	
25	DB	IN←IOFF
26	FF	
27	E6	ANi 01
28	01	
29	C2	JNZ→0025
2A	25	
2B	00	
2C	C3	JMP→0003
2D	03	
2E	00	

HEXADECIMAL EXAMPLE

Data Switches								
Data	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0
00 =	0	0	0	0	0	0	0	0
01 =	0	0	0	0	0	0	0	1
02 =	0	0	0	0	0	0	1	0
03 =	0	0	0	0	0	0	1	1
04 =	0	0	0	0	0	1	0	0
05 =	0	0	0	0	0	1	0	1
06 =	0	0	0	0	0	1	1	0
07 =	0	0	0	0	0	1	1	1
08 =	0	0	0	0	1	0	0	0
09 =	0	0	0	0	1	0	0	1
0A =	0	0	0	0	1	0	1	0
0B =	0	0	0	0	1	0	1	1
0C =	0	0	0	0	1	1	0	0
0D =	0	0	0	0	1	1	0	1
0E =	0	0	0	0	1	1	1	0
0F =	0	0	0	0	1	1	1	1
10 =	0	0	0	1	0	0	0	0
...etc....								

NOTE: Color caps have been included in the kit to color code the switches either in an octal or hexadecimal format.

OCTAL =	S_9S_6	$S_5S_4S_3$	$S_2S_1S_0$
	X X	0 0 0	X X X
HEX =	$S_7S_6S_5S_4$	$S_3S_2S_1S_0$	
	X X X X	0 0 0 0	

BYT-8 FRONT PANEL BOARD

Parts List

PART NUMBER	QTY	PART DESCRIPTION
00011-005	14	.1 ufd, 15 v, ceramic capacitor, C3, C4, C7-C18
00011-002	2	.001 ufd, 25 v, ceramic capacitor, C5 & C6
00015-007	2	33 ufd, 25 v, dipped tantalum capacitor, C1 & C2
00025-002	1	Diode, silicon, 1N914, CR1
00027-001	1	Heat sink, 1.2" x 1", Q1
00033-001	1	+5 v regulator, 7805C, Q1
00045-002	4	IC, 74LS02N, B14, C10, C13, D3
00045-003	11	74LS367N, A15, A16, B8, B16, C12, C16, D10-D14
00045-004	6	74LS00N, B6, B9, C1, C2, C3, D4
00045-005	3	74LS04N, B7, B10, C9
00045-006	3	74LS30N, C11, D1, D15
00045-009	1	8212D, C15
00045-019	2	7405N, B17 & C17
00045-017	1	74LS08N, C8
00045-016	2	7410N, D8 & D9
00045-020	4	7486N, B11-B13, B15
00045-021	1	7420N, C6
00045-014	3	74LS107N, C4, C7 & D2
00045-015	1	74LS123N, C5
00048-001	1	Hex nut, 4-40
00069-003	16	Toggle switch, ON-ON, S0-S15
00069-004	6	Toggle switch, (ON)-OFF-(ON), S17-S22, (MOMENTARY)
00069-005	1	Toggle switch, ON-OFF-ON, S16
00076-001	1	Internal lock washer, #4
00085-001	17	Resistor, 220 ohm, 1/4 w, 5%, R34-R49, R29 (red, red, brwn)
00085-004	31	Resistor, 1K ohm, 1/4 w, 5%, R1-R28, R31, R32, R50 (brwn, blk, red
00085-010	1	Resistor, 270K ohm, 1/4 w, 5%, R51 (red, vlt, yel)
00085-009	1	Resistor, 47K ohm, 1/4 w, 5%, R33 (yel, vlt, org)
00085-011	1	Resistor, 100K ohm, 1/4 w, 5%, R30 (brwn, blk, yel)
00145-001	17	LED, LEDØ-LED16
00153-001	1	BHMS, 4-40 x 3/8
00184-002	1	Connector socket, 16 pin, J1
00184-004	1	Connector socket, 24 pin, C15
10001-011	1	PCB, C1000-1011 Assembly, Rev. B
61112-002	1	Front panel (optional)