

BYTE MPU BOARD

FUNCTIONAL DESCRIPTION

The BYTE MPU Board controls and processes all instructional data within the BYT-8 Computer. It features an 8080A microprocessor, a crystal controlled clock generator, a vector interrupt circuit, and contains eight input (DIØ-7) and eight output (DOØ-7) lines to and from the motherboard (S-100 bus), and logic control circuits. A functional block diagram is shown in Figure 3.

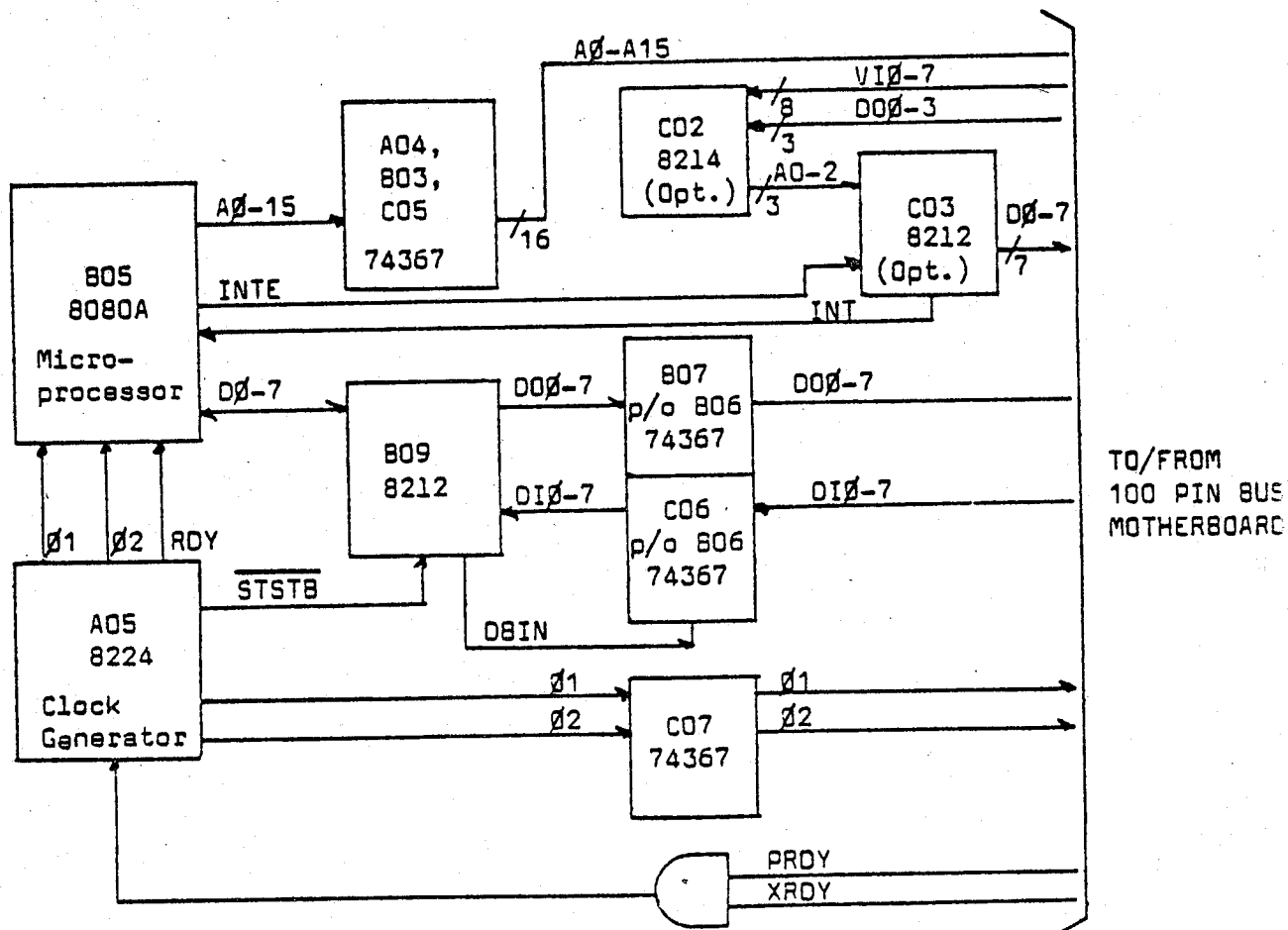


FIGURE 3. Functional Block Diagram for the MPU Board

THEORY OF OPERATION

The primary feature of the MPU Board is the 8080A microprocessor IC; most of the Board provides support for this unit. The MPU Board interfaces between the 8080A and the data and address buses, block and timing signals, and the necessary voltage regulation for the 8080A and the other ICs. (The internal operation of the 8080A is covered in the user's manuals available from the various manufacturers.)

The 16 address lines from the 8080A drive the address bus (A₀-15) through A04, A03, and C05 (three 74367 or equivalent IC's). The 74367's are tri-state buffer drivers. They are disabled through the ADD DSBL line on pin 22. Three more 74367's, B06, B07, and C06, are connected as the DATA IN (DI₀-7) and DATA OUT (DO₀-7) bus drivers. The DATA OUT buffers are controlled by the DO DSBL signal on pin 23. The data bus is also connected to J1, the data bus socket, and to the status byte latch, B09 (8212). The data bus socket connects the front panel to the data bus. The latch, B09, transfers the Status Byte to the 100-pin motherboard through C07 and C09 (two 74367's). These two 74367's are disabled by the STAT DSBL signal at pin 18. The 8212 (B09) is latched by the STSTRB signal from A05 pin 7 to store the status data for each instruction cycle.

A resistor array (A08) consisting of eight 4.7k ohm resistors is connected to the bidirectional data bus lines to ensure that during the time when the bus is not being driven, the 8080A reads all 1's. The clock generator IC, A05 (8224), and external crystal (Y1) form a two-phase nonoverlapping 2 MHz system clock circuit for the 8080A. The two-phase clock is also provided through the 100-pin connector to the motherboard by way of C07 (74367). The CLOCK line (pin 49) of the motherboard is driven from the ϕ 2 TTL output (A05 pin 6) through a series of six inverters to provide a delay so that the phase relationship of the CLOCK signal to the ϕ 1 and ϕ 2 clocks on the motherboard is almost

identical to that produced by the MITS Altair 8800 system. The A05 (8224) also provides the power-on reset function through the use of a 4.7k ohm resistor (A08) and a 33 uf capacitor (C30) connected to the RESIN input of A05 pin 2. The RS (Reset) output of A05 pin 1 is applied to the motherboard as the POC (pin 99), Power-On Clear signal.

The PRDT (pin 72) and XRDY (pin 3) signals are ANDed before being applied to the RDYIN input of A05 pin 3 to be synchronized with the $\phi 2$ clock before being applied to 805 (8080A). The PINT signal (pin 73) is connected through an inverter to 803 pin 14 (74367) and goes out pin 13 of 803 to pin 14 (INT) of 805 (8080A). The PHOLD signal (pin 74) is synchronized with the $\phi 2$ clock in the D flip-flop (A03) before being applied to pin 12 of 803 and goes out pin 11 of 805 pin 13 (HOLD).

The six processor status signals (PSYNC, PWR, PDBIN, PINTE PHLDA, and PWAIT) are applied to the motherboard through C04 (74367). This buffer is disabled by the CCDSBL signal (pin 19).

The +5 vdc is regulated by Q2 and Q3 (two 7805's) from the +8 vdc unregulated supply at pins 1 and 51. The -5 vdc is regulated by Q4 (79L05) from the -16 vdc unregulated supply at pin 52. The +12 vdc is regulated by Q1 (74L12) from the +16 vdc unregulated supply at pin 2. All three regulated supplies are filtered by 33 uf capacitors and by 0.1 uf disc capacitors.

Vectored Interrupt Circuit

The Vectored Interrupt Circuit consists of C02 (8214), a priority interrupt controller, C03 (8212), an eight-bit input/output port, and associated pull-up resistors.

The 8214 (C02) is basically an eight-level priority control unit that accepts eight different interrupt requests, determines which has the highest priority, compares the new interrupt level to a software controlled current status register, and issues an interrupt to the system based on this comparison with

vector information to locate the service routine. The highest priority interrupt is VI7 and the lowest is VI0. When an interrupt request (INTE) is presented to CO2 pin 7 (8214), it issues an interrupt to 805 (8080A) pin 14, if the Vectored Interrupt Circuit is enabled (INTE signal from 805 pin 16). The interrupt request is encoded into three bits (modulo 8) $\overline{A0}$, $\overline{A1}$, and $\overline{A2}$, are applied to CO3 (8212). After the interrupt has been acknowledged by 805 (8080A), the encoded RST (Restart) instruction is gated onto the bidirectional data bus by CO3 (8212). The processor executes the instructions and points the program counter to the desired service routine.

The $\overline{INT}$ signal (CO2 pin 5) is applied to CO3 pin 11 (STB) so that proper timing is maintained. The 8212 (CO3) is enabled when the INTA and DBIN signals from 805 (8080A) are active, thus ensuring that the RST instruction is placed on the bidirectional data bus at the proper time.