

BYTE FRONT PANEL BOARD

FUNCTIONAL DESCRIPTION

The Front Panel Board provides buffering for all the front panel switches and receives the information to be displayed by the LED's on the front panel. The CPU control circuits are located on this board. The board also provides the necessary circuits to produce twelve switch-selectable functions, can selectively display 16-bits (two 8-bit bytes) of Machine Address, one byte of CPU Status and one byte of CPU Data, one byte of Machine State and one byte of I/O Port Data, protect or not protect the contents of memory, examine and/or modify the contents of memory, set or reset the RUN latch, single instruction step, stop on any OP Code Address Compare, and Input Port can sense eight switches (front panel), reset front panel and CPU, or reset entire system except the CPU. See Figure 1.

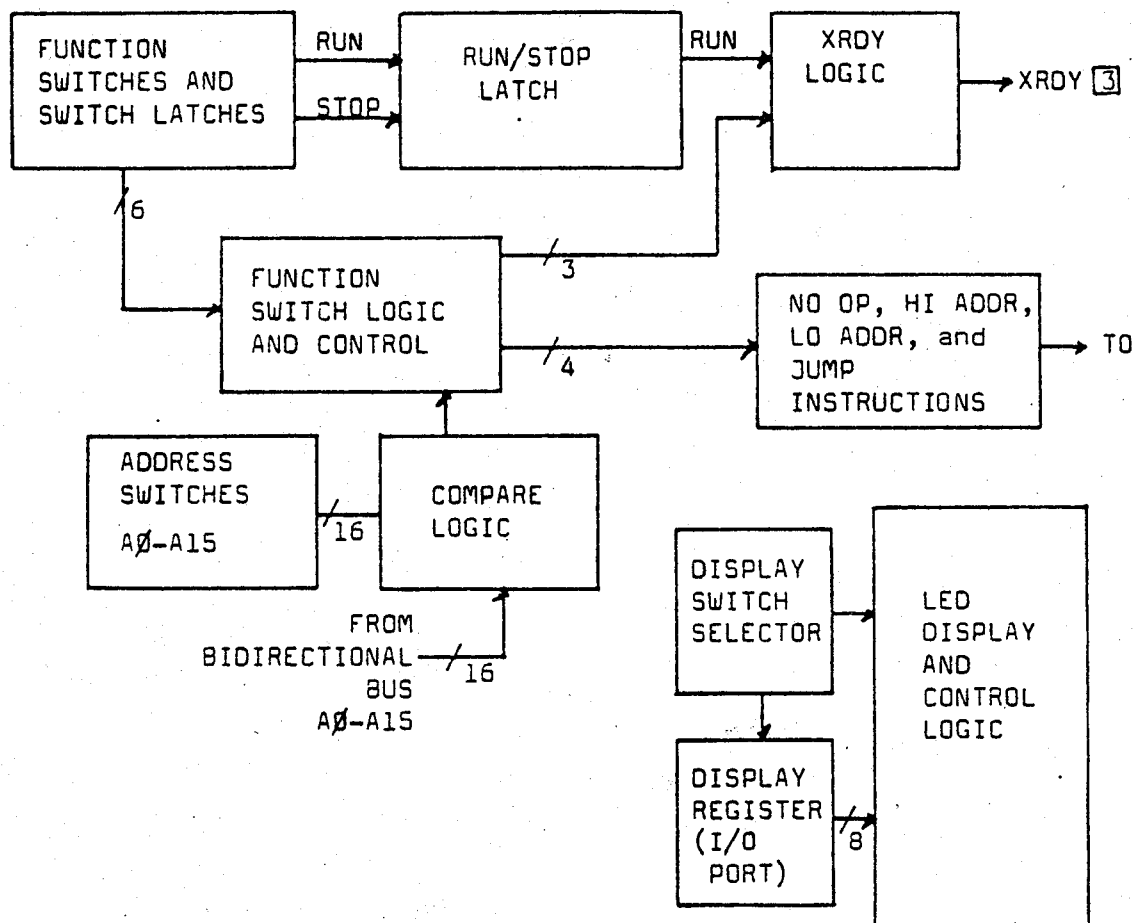


FIGURE 1. BYT-8 Front Panel Board Simplified Block Diagram

THEORY OF OPERATION

The six Front Panel function switches (S17-S22) allow the operator to control the CPU. The CPU is controlled by the XRDY line 3, the SS (Single Step) line 21, and the RUN line 71, all of which are produced from the Front Panel Board. Refer to the Front Panel Switches and Displays photograph, pg. 4, and the Overall Schematic Diagrams.

RUN/STOP Functions

The RUN/STOP switch, S17, controls the XRDY line through the RUN/STOP latch. The RUN/STOP latch is actually two separate latches (RUN and STOP) that are interconnected to produce the RUN/STOP latch functions. (See Figure 2.) The RUN function is initiated by setting the RUN/STOP switch to the RUN position. This generates a negative 100us pulse ($\overline{\text{SET RUN}}$) that is applied to D1 pins 4, 5, and 6 and to B6 pin 2. The negative-going edge of the pulse from D1 pin 8 triggers a 3 ms negative pulse from C5 pin 4 ($\overline{\text{DEBOUNCE SS}}$). The low signal ($\overline{\text{SET RUN}}$) at B6 pin 2 causes B6 pin 3 to go high and hold D8 pin 4 high. D8 pin 5 is held high because $\overline{\text{RESET}}$ is high at this time. D8 pin 3 is held high because B6 pin 4 ($\overline{\text{DEBOUNCE SS}}$) is low, forcing B6 pin 6 to go high. D8 pin 6 is low and B6 pin 1 is held low, the RUN latch is now set and the low ($\overline{\text{SET RUN}}$) input signal at pin 2 can be removed without affecting the latch. The low at D8 pin 6 causes C10 pin 3 to be low. The low at B6 pin 8 (STOP) holds C10 pin 2 low and this allows C10 pin 1 (RUN) to go high. The high from C10 pin 1 is inverted at B10 pin 2 ($\overline{\text{RUN}}$) and applied to C6 pin 1. If the Front Panel is not in an Examine, Examine Next, or STEP function, the other three inputs to C6 will be high and C6 pin 6 will go high. This signal is buffered by B8 and produced at B8 pin 5 (XRDY, bus pin 3). The high on the XRDY line puts the CPU into a RUN operation. The $\overline{\text{DEBOUNCE SS}}$ signal at B6 pin 4 goes high after 3 ms delay, but B6 pin 5 remains low, holding B6 pin 6 high. The RUN/STOP latch will remain set until the $\overline{\text{SET STOP}}$ or the $\overline{\text{RESET}}$ signal goes low.

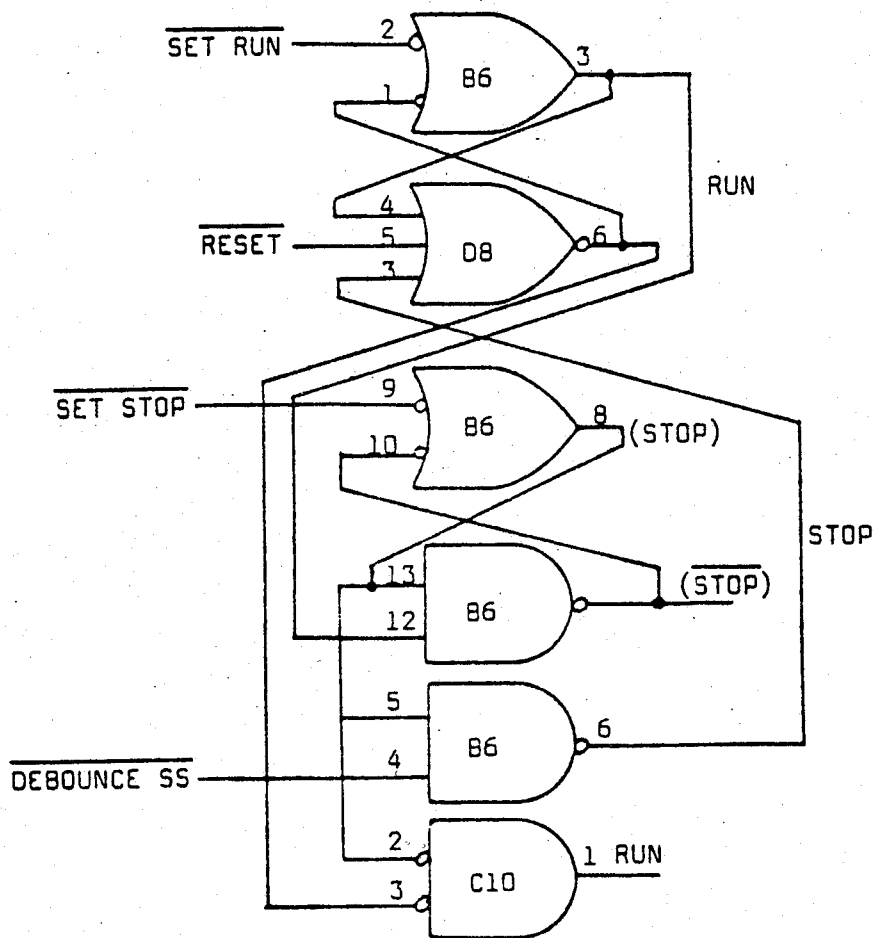


FIGURE 2. RUN/STOP Latch Simplified Schematic

The STOP function is initiated by setting the RUN/STOP switch, S17, to the STOP position. This generates a negative 100 us pulse that is applied to D4 pin 13 and causes D4 pin 11 to go high. This high is applied to C6 pin 9. C6 pin 10 is high (PSYNC), pin 12 is high ($\emptyset 2$), and pin 13 (SM1, Machine Cycle 1 - fetch cycle) is high. So C6 pin 8 goes low (SET STOP). This signal causes B6 pin 8 (STOP) to go high and holds B6 pins 5 and 13 high and C10 pin 2 high. B6 pin 11 goes low and holds B6 pin 10 low, setting the STOP latch. B6 pin 6 can now go low and cause D8 pin 6 to go high and reset the RUN latch. The high on D8 pin 6 inhibits the RUN signal (C10 pin 1). The RUN/STOP latch will remain in this state, SET RUN signal is received at B6 pin 2, and the RUN/STOP latch cycle starts over.

Examine Function

The Examine function is initiated by setting switch S22 (EXMN/ENXT) to the EXMN position, generating a 100 ms negative-going pulse that is applied to C1 pin 1 and D1 pin 12. The positive-going pulse at D1 pin 8 triggers a 3 ms pulse from C5 (a monostable flip-flop) on its negative transition. The 3 ms pulse removes the low (0) from the latch circuits and allows C1 pin 6 to go low (0). This 3 ms time delay removes any switch bounce from the output signal. The low signal from C1 pin 6 is applied to D3 pin 2. 89 pins 9 and 10 are held high by the $\overline{Q}$ outputs of C7 pins 2 and 6. The low output of 89 pin 8 is applied to D3 pin 3, allowing the output pin 1 to go high. The high output of C9 pin 12 holds the output of D3 pin 4 low. The input at D3 pin 12 causes the output (pin 13) to go low. This negative transition applied to C7 pin 12 causes the J-K flip-flop to toggle, causing the Q and $\overline{Q}$ outputs to change state (pin 3 is high and pin 2 is low). The two J-K flip-flops are connected as a Two Bit Counter (four states). The change in the outputs of the first flip-flop has no effect on the second flip-flop. But the input to 89 pin 10 is now low and the output of 89 pin 8 is high, causing pin 1 of D3 to go low and C9 pin 12 to go low and hold pin 6 of D3 low. The high at C7 pin 3 (Q) is applied to C7 pin 9 and to D9 pins 5 and 10. The high at C7 pin 6 is applied to D9 pin 9 and to 89 pin 9. The PDBIN signal at C9 pin 6 goes high and is applied to D9 pin 11, causing D9 pin 8 to go low and C9 pin 10 to go high (JMP). This enables the JUMP instruction (C3 HEX 11000011) to be applied to the bidirectional bus through J1 via the inverters in B17 (pins 1, 9, 11, and 13).

The PSYNC signal (76) is inverted at 87 pin 2, buffered by 88, and applied to various circuits from C8 pin 3 as $\overline{\text{PSYNC}}$. $\overline{\text{PSYNC}}$ is applied to D3 pin 5 and with pin 6 held low, the output (pin 4) goes high. This pulse going positive causes D3 pin 13 to go low and trigger the J-K flip-flop (C7) a second time.

This causes the output at pin 3 to go low and at pin 2 to go high. The low-going signal from pin 3 causes the second J-K flip-flop to change state, pin 5 goes high and pin 6 goes low. The change in the outputs of the flip-flops causes D9 pin 8 to go high, inhibiting the JUMP instruction (C3 HEX). D8 pins 2 and 13 are held high so the next PDBIN signal causes D8 pin 12 to go low and puts the GATE LO ADDRESS signal from C8 pin 8 on A16 pins 1 and 15 and on B16 pin 15. This allows the eight low address bits (A0 through A7) to be placed on the bidirectional bus by the 74367's. The 74367's are 3-state logic 6-bit noninverting buffers (see the description of 3-state logic).

The second PSYNC pulse causes C7 pin 12 to go low and change the output states a third time, pin 3 goes high and pin 2 goes low. The second J-K flip-flop does not change state, so pin 5 remains high and pin 6 remains low. D8 pin 12 goes high, inhibiting the GATE LO ADDRESS signal. D9 pins 3 and 5 are high and the next PDBIN pulse causes pin 6 to go low and the GATE HI ADDRESS signal enables A15 pin 1 and B16 pin 1. This allows the eight high addresses (A8 through A15) to be applied to the bidirectional bus.

The third PSYNC pulse again causes the trigger input of C7 (pin 12) to go low and change the state of the outputs, pin 3 goes low and pin 2 goes high. The change of state at pin 3 causes the second J-K flip-flop to change state, pin 5 goes low and pin 6 goes high. Both J-K flip-flops are back to their original states. The GATE HI ADDRESS is inhibited when D9 pin 6 goes high.

The Examine function logic has provided the CPU with a JUMP instruction and the two address bytes (high and low) that the CPU expects after a JUMP instruction. The CPU is halted during the fetch routine for the addressed memory byte.

Deposit Function

The Deposit function is initiated by setting switch S21 (DEP/DNXT) to the DEP (Deposit) position, generating a 100 ms negative-going pulse that is applied

to D1 pin 2 and to C3 pin 13. The positive-going pulse at D1 pin 8 triggers a 3 ms pulse from C5 pins 4 and 13 on its negative transition. The 3 ms pulse removes any switch bounce from the output of the latches. The low at C3 pin 8 is applied to C8 pin 1 and C8 pin 2 is held high. Therefore, the output of C8 (pin 3) goes low and triggers D2 (J-K flip-flop) that has been reset by C5 pin 13 returning to a low. D2 pin 3 is now high and is applied to D4 pins 10 and 5. D2 pin 6 is set high by the last $\overline{\text{PSYNC}}$ pulse and is applied to D4 pin 9. The output of D4 (pin 8) goes low and triggers a 15 ms negative pulse from C5 pin 12. This pulse is applied to B9 pin 2. Pin 1 of B9 is the $\overline{\text{PWR}}$ signal (Processor Write). The output of this gate is ANDed with C8 pin 4 ($\overline{\text{SOUT}}$) to produce the $\overline{\text{MWRITE}}$ signal (68). The $\overline{\text{PWAIT}}$ (27) signal at D4 pin 4 causes D4 pin 6 to go low. This produces the $\overline{\text{GATE DATA}}$ signal that is applied to D8 pin 11 and to C8 pin 10. Pin 8 of C8 goes low, producing the $\overline{\text{GATE LO ADDRESS}}$ signal to apply the eight bits of data to the bidirectional bus. D8 prevents the CPU from applying data on the bidirectional bus while the Front Panel is inserting data. The inputs to D8 are as follows: pin 11 - $\overline{\text{GATE DATA}}$; pin 10 - the output of B9 pin 8 is low only during the time that both C7's flip-flops are reset; and pin 9 - low only when D2 pin 9 has been triggered and pin 8 is high (this occurs during either the Examine Next or Deposit Next function). The output of D8 (pin 8) then goes high, causing B7 pin 10 to go low, holding both (21) and (71), SS and RUN, low.

Examine Next Function

The Examine Next function is initiated by setting the EXMN/ENXT switch S22 to the ENXT position. This produces a low at C1 pin 8 after a 3 ms delay as previously described. This low is applied to C2 pin 10 and causes a high from C2 pin 8. This high is inverted by B7 and applied to D2 pin 9. If the processor is halted, pin 8 of D2 will be high ($\overline{\text{RUN}}$) and pin 6 will go low.

The signal from pin 6 is applied to D3 pin 9 and to C6 pin 4. D3 pin 10 goes high with the next PDBIN signal to produce a NO OP instruction (000 HEX) to be applied to the bidirectional bus and to gate out the XRDY signal from C6 pin 6. PSYNC resets D2 pin 6 to a high on the next pulse. This removes the low on D3 pin 9 and removes the NO OP instruction from the bus.

Deposit Next Function

The Deposit Next function is initiated by setting the DNXT/DEP switch S21 to the DNXT position. After a 3 ms delay, a high is produced at pin 3 of C2 and a low at pin 6 of C2. The low at pin 6 is applied to pin 9 of C2. This signal follows the same path as the Examine Next function previously described, generating a NO OP instruction and gating out the XRDY signal. The high from pin 3 follows a different path and generates different signals. The high is applied to C2 pin 12 and pin 13 is set high on the PSYNC pulse, causing pin 11 of C2 to go low. This low-going pulse is ORed through C8 and applied to D2 pin 12. The low-going edge triggers the J-K flip-flop, if pin 1 (RUN) is high. This causes the output of D2 (pin 3) to go high. The signal at pin 3 is applied to D4 pins 5 and 10. The signal at pin 4 of D4 is PWAIT and causes D4 pin 6 to go low, producing the GATE DATA signal. This signal is applied to C8 pin 10 to generate the GATE LO ADDRESS instruction that enables A16 and part of B16. The GATE DATA signal is also applied to D8 pin 11 to hold SS and RUN signals low.

When D2 pin 6 is high and D2 pin 3 is high, D4 pin 8 goes low, triggering a 15 us negative pulse from C5 pin 12. This signal produces the MWRITE signal when gated with PWR and SOUT signals as described in the Examine Next function. The next PSYNC signal inhibits the NO OP instruction by resetting D2 pin 10.

Step Function

The Step function is initiated by setting the STEP/CMPR switch, S21, to the STEP position. After a 3 ms delay, C3 pin 6 goes low, causing C4 pin 6 to go low, if pin 8 ($\overline{\text{RUN}}$) is high. The signal from pin 6 is $\overline{\text{STEP}}$. This is applied to C6 pin 2 to produce the XRDY signal. The next PSYNC signal resets C4 pin 6 to a high.

Set Compare Stop Function

The Set Compare Stop function is initiated by setting the STEP/CMPR switch, S20, to the CMPR position. The switch closing produces a negative-going pulse at C4 pin 12, that causes C4 pin 3 to go high. This high is applied to D4 pin 2. D4 pin 1 is high when D15 pin 8 goes low, and B10 pin 12 goes high when the programmed and selected addresses compare. Then pin 3 of D4 goes low and is applied to D4 pin 12. D4 pin 11 goes high and is applied to C6 pin 9. C6 pin 10 is PSYNC, pin 12 is $\phi 2$ clock, and pin 13 is SM1 (Machine Cycle 1 — fetch cycle). When all four signals are high, C6 pin 8 goes low, producing the $\overline{\text{SET STOP}}$ signal, that is used to set the RUN/STOP latches to STOP. When the latch is set to stop, the $\overline{\text{STOP}}$ signal from B6 pin 11 resets C4 pin 3 to a low.

Input/Output Port Functions

The lower eight switches (S8-S15) are used for the address of the I/O Port functions. The upper switches are also used as sense switches. The inputs to C11 are the eight upper addresses (A8-A15 or FF HEX); when all eight are low, C11 pin 8 is low ($\overline{\text{ADDR=FF}}$). This signal is applied to C9 pin 9, inverted and available at pin 8. The signal from pin 8 is applied to D9 pin 13. It is ANDed with SINP on pin 2 and with PDBIN on pin 1. When all three signals are high, pin 12 goes low. This produces the $\overline{\text{SSWDSB}}$ signal (Status Word Disable) (53), that is gated to prevent timing problems on the bidirectional bus from the CPU and the Front Panel Board. The other place that this signal is applied

is to C8 pin 12. This signal causes pin 8 to go low and produce the Gate Hi Address signal. The Gate Hi Address signal enables A15 and B16 bus drivers. This allows the upper address switches to be placed on the bidirectional bus without interference from the CPU.

The signal from C11 pin 8 ($\overline{ADDR=FF}$) is applied to C10 pin 6 and is ANDed with $\overline{SOUT}$. When both signals are low, pin 4 goes high and B10 pin 8 goes low. This signal holds C10 pin 9 low. C10 pin 8 goes low when $\overline{PWR}$ (Processor Write) is low. This causes pin 10 to go high and applies a high to C15 pin 11 (Strobe). With the DISPLAY SELECTOR switch (S16) in the center position, B9 pin 11 is low and holds C15 pin 13 high. When pin 13 is high, the eight outputs of C15 are enabled. The high at pin 11 latched in the data from the eight input lines. Whenever the DISPLAY SELECTOR switch is in either the up or down position, B9 pin 11 will be high, forcing C15 pin 13 low, disabling the eight outputs of C15.

When the DISPLAY SELECTOR switch is in the down position, C12 pin 1, D12 pins 1 and 15, and D11 pins 1 and 15 are enabled so the 16-bits of address are displayed ($A0-A15$). When the DISPLAY SELECTOR is in the center position, B9 pin 11 is low and C15 pin 12, D13 pin 15, and D10 pins 1 and 15 are enabled so that 8-bits of state and 8-bits of I/O Port are displayed. When the DISPLAY SELECTOR is in the up position, C12 pin 15, C16 pin 1, D13 pin 1, and D14 pins 1 and 15 are enabled so that 8-bits of data and 8-bits of status are displayed.

Reset/Clear Functions

The Reset/Clear functions are initiated by setting S18 (CLR/RESET) to the desired position. The RESET position forces the $\overline{RESET}$ line low (75), resetting C5, C7, the RUN/STOP latch, and C15. The signal is also applied to the CPU where it resets the program counter to 0 000 000 000 000 000, the first memory address. This is a quick way to get back to the first step of a program,

if it begins at the first memory address. The CLR position produces the same effect as the RESET position, with the extra function that it will clear all the external input and output devices. Whenever the switch (S18) is set to RESET, a CLR signal is produced because of the diode (CR1) connecting the $\overline{\text{RESET}}$ line to the $\overline{\text{CLR}}$ line.

Protect/Protect Functions

The Protect/Protect functions are initiated by setting S19 (PROT/ $\overline{\text{PROT}}$) to either desired position. In the PROT position, when $\overline{\text{RUN}}$ is high, the PROT line (70) is set high; this signal is applied to the memory protection circuits and prevents any change in the contents of memory. When the switch is set to the $\overline{\text{PROT}}$ position, when $\overline{\text{RUN}}$ is high, the $\overline{\text{PROT}}$ line (20) is set high; this will disable the memory protection circuits and allow the memory contents to be changed.